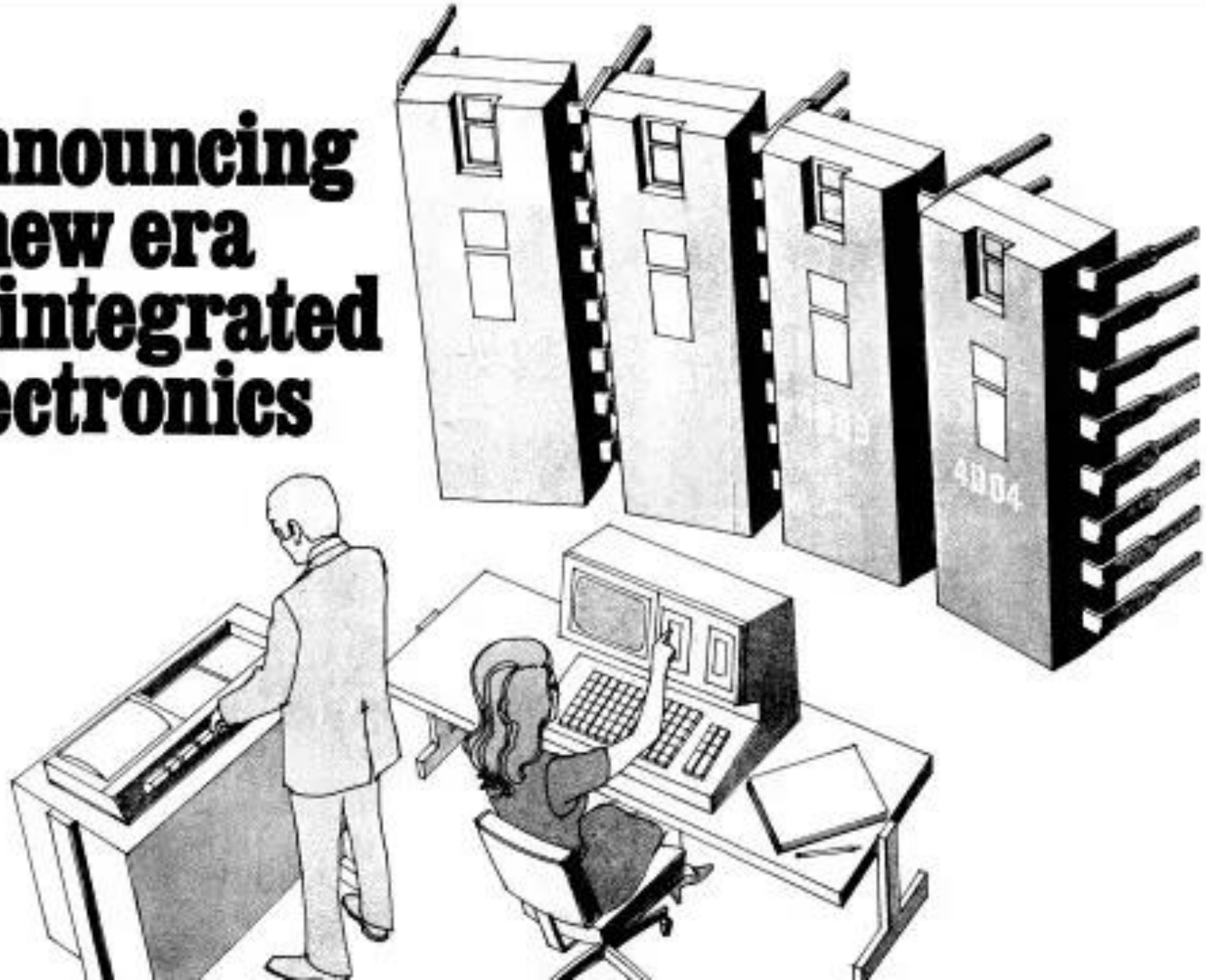
“system on a chip” (SoC)

Announcing a new era of integrated electronics



A micro-programmable computer on a chip!

Intel introduces an integrated CPU complete with a 4-bit parallel adder, sixteen 4-bit registers, an accumulator and a push-down stack on one chip. It's one of a family of four new ICs which comprise the MCS-4 micro computer system — the first system to bring you the power and flexibility of a dedicated general-purpose computer at low cost in as few as two dual in-line packages.

MCS-4 systems provide complete computing and control functions for test systems, data terminals, billing machines, measuring systems, numeric control systems and process control systems.

The heart of any MCS-4 system is a Type 4004 CPU, which includes a powerful set of 45 instructions. Adding one or more Type 4001 ROMs for program storage and data tables gives you a fully flexible micro-programmed computer. To this you may add Type 4002 RAMs for read-write memory and Type 4003 registers to expand the output ports.

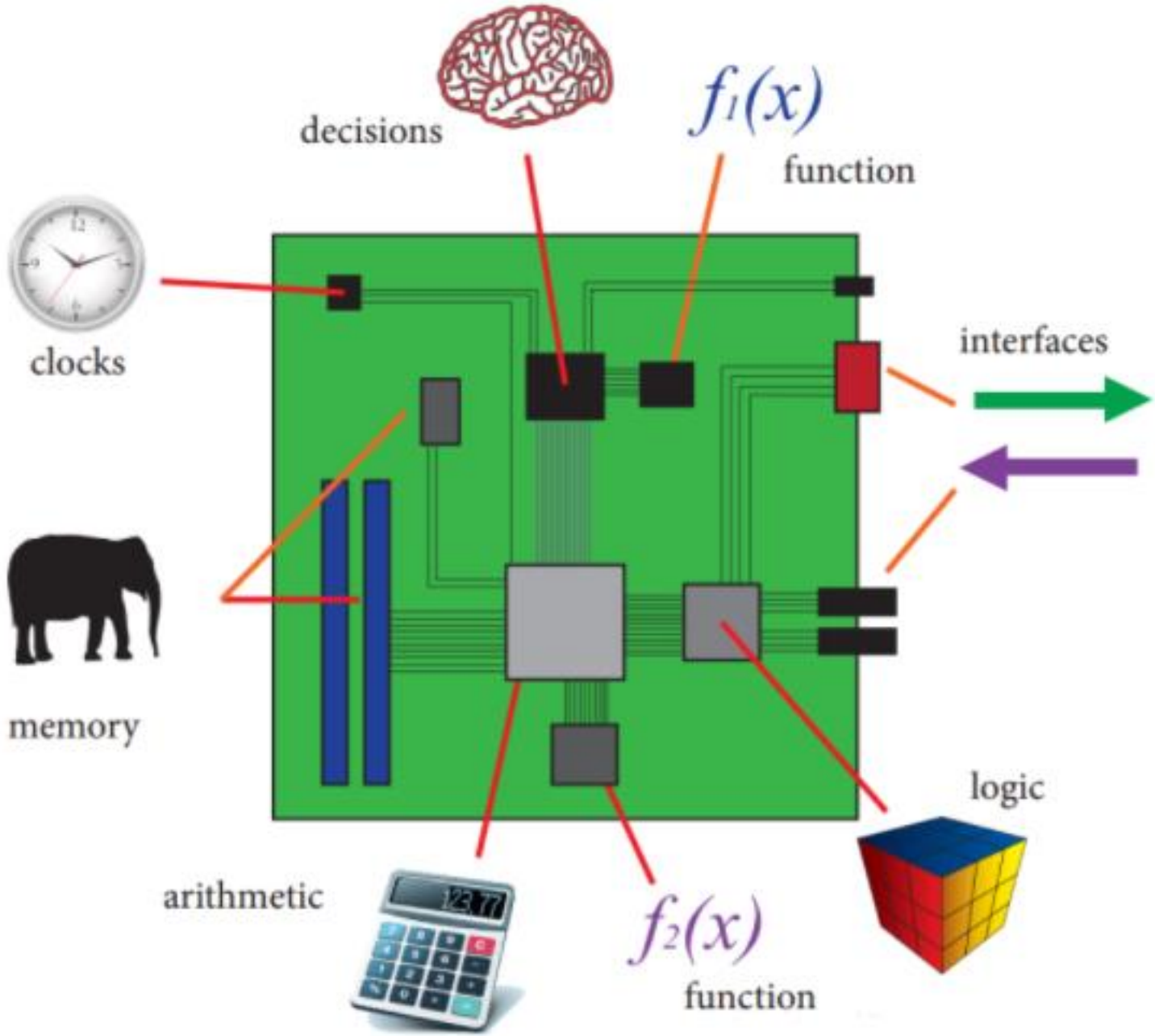
Using no circuitry other than ICs from this family of four, you can create a system with 4096 8-bit bytes of ROM storage and 5120 bits of RAM storage. When you require rapid turn-around or need only a few systems, Intel's erasable and re-programmable ROM, Type 1701, may be substituted for the Type 4001 mask-programmed ROM.

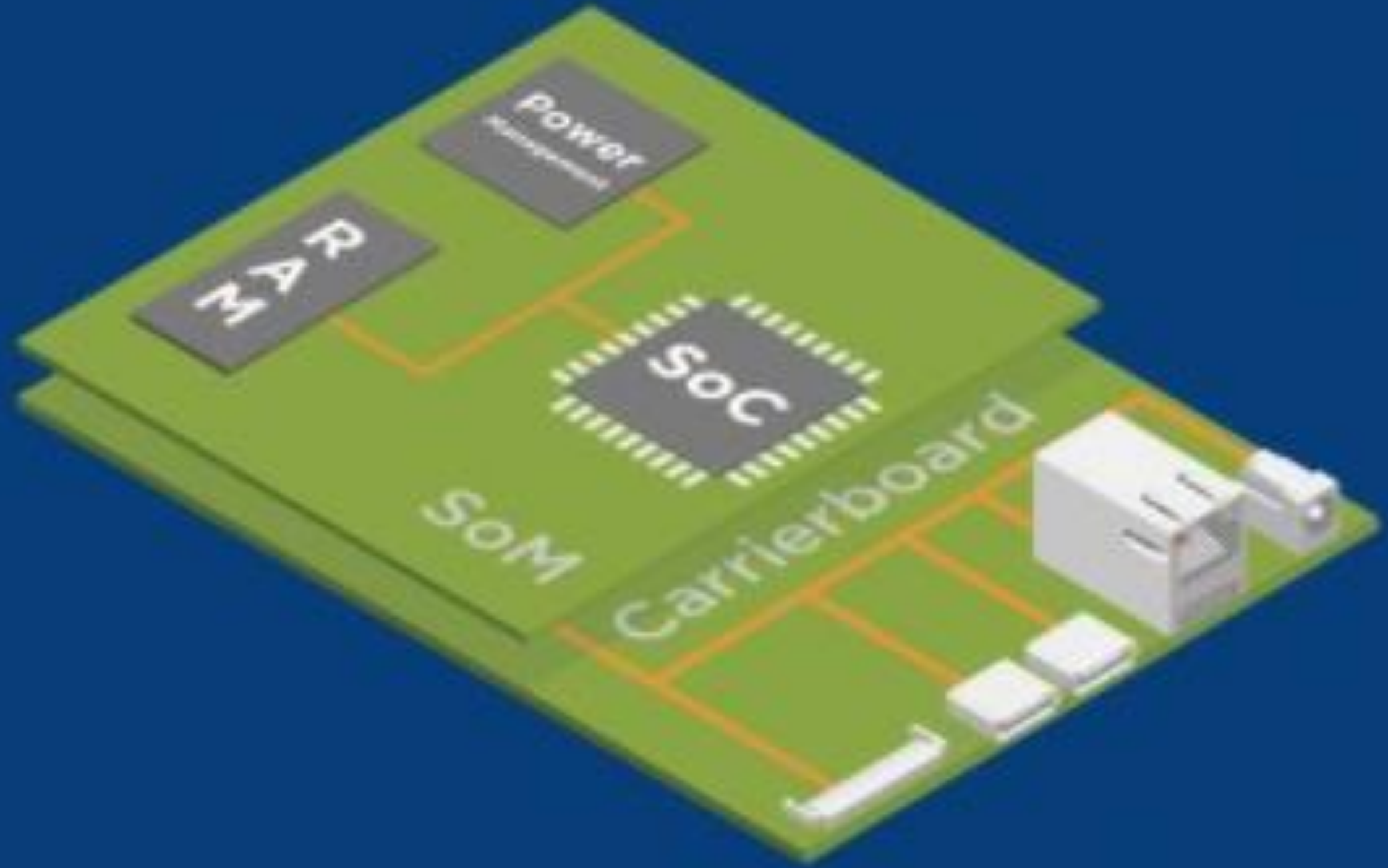
MCS-4 systems interface easily with switches, keyboards, displays, teletypewriters, printers, readers, A-D converters and other popular peripherals.

The MCS-4 family is now in stock at Intel's Santa Clara headquarters and at our marketing headquarters in Europe and Japan. In the U.S., contact your local Intel representative for technical information and literature. In Europe, contact Intel at Avenue Louise 210, B 1050 Bruxelles, Belgium. Phone 462003. In Japan, contact Intel Japan, Inc., Parkside Flat Bldg. No. 4-2-3, Sendagaya, Shibuya-Ku, Tokyo 151. Phone 03-423-4747.

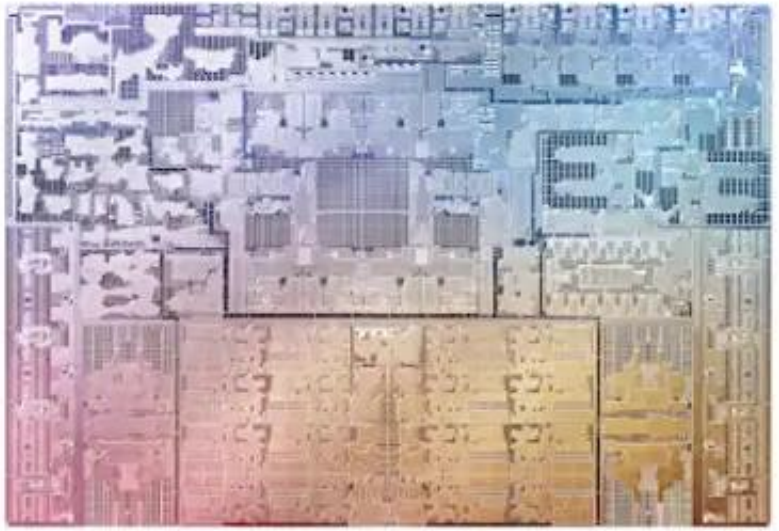
Intel Corporation now produces micro computers, memory devices and memory systems at 3065 Bowers Avenue, Santa Clara, Calif. 95051. Phone (408) 246-7501.

intel®

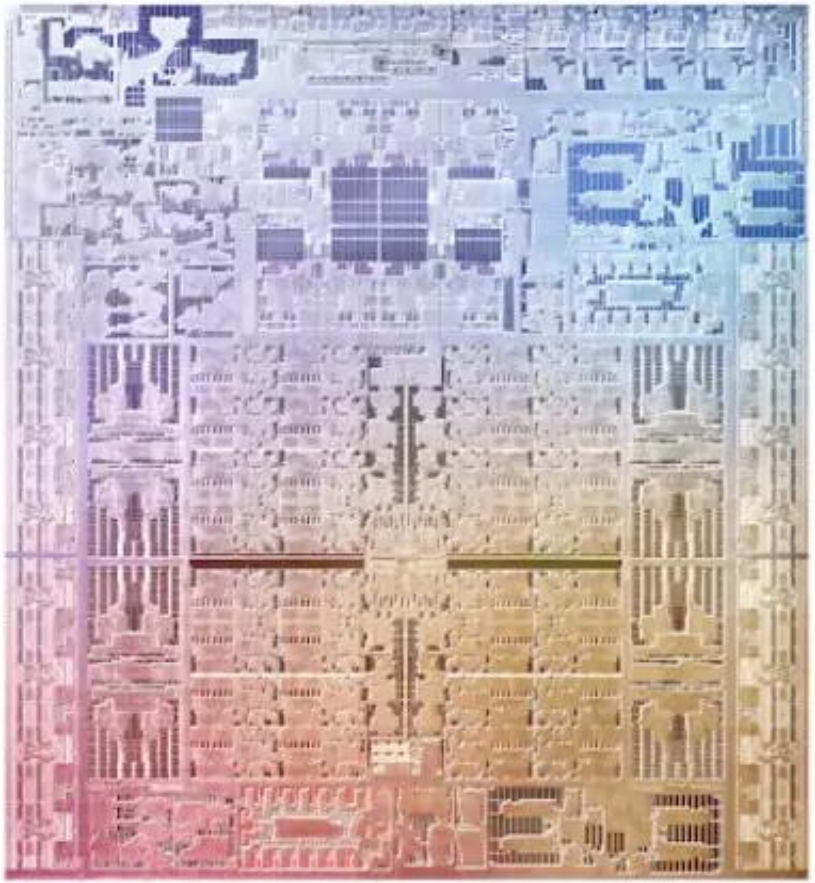

decisions
$f_1(x)$
function
clocks
interfaces
memory
logic
arithmetic
$f_2(x)$
function


Power
RAM
SoC
SoM
Carrierboard

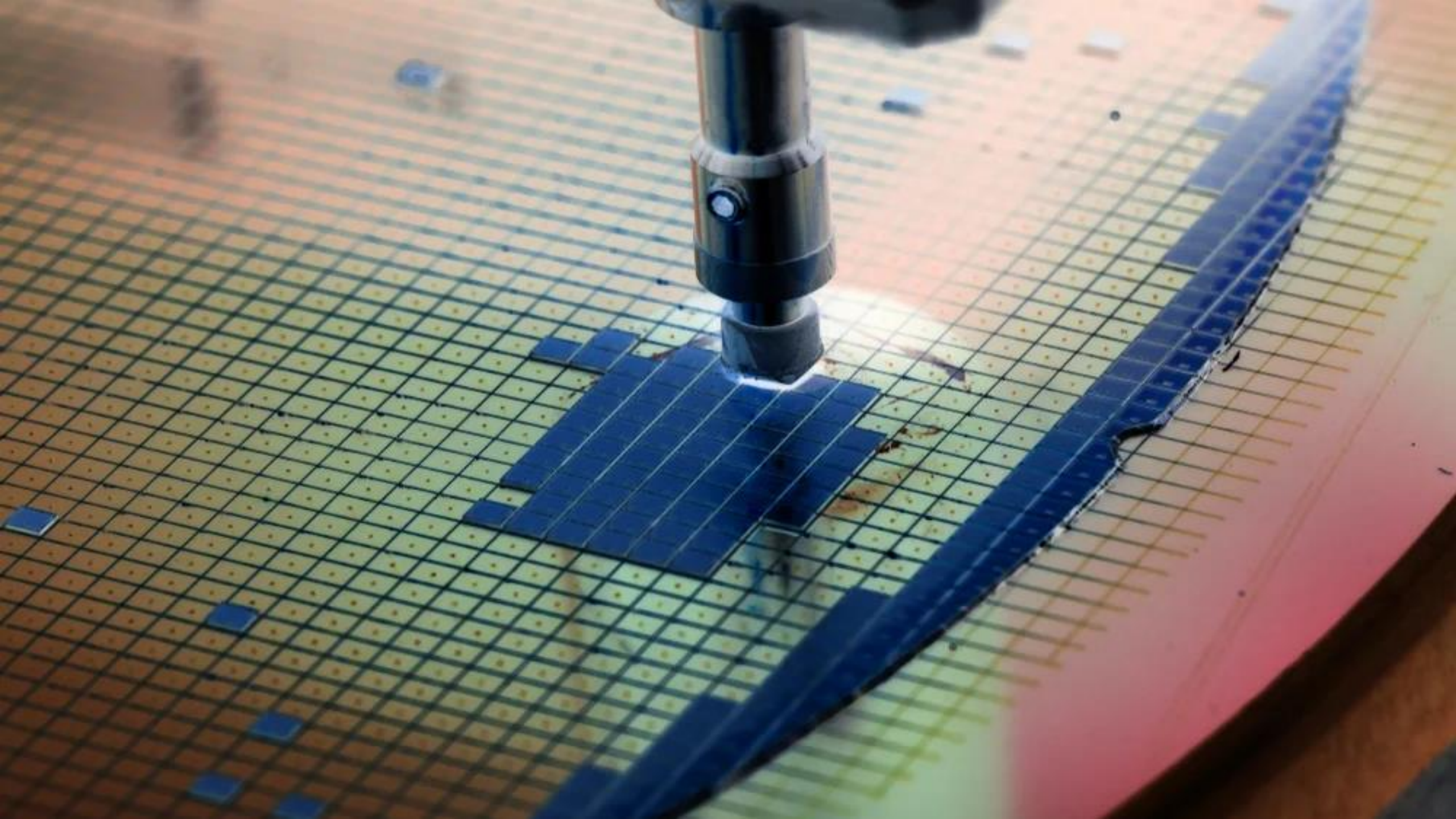
M1

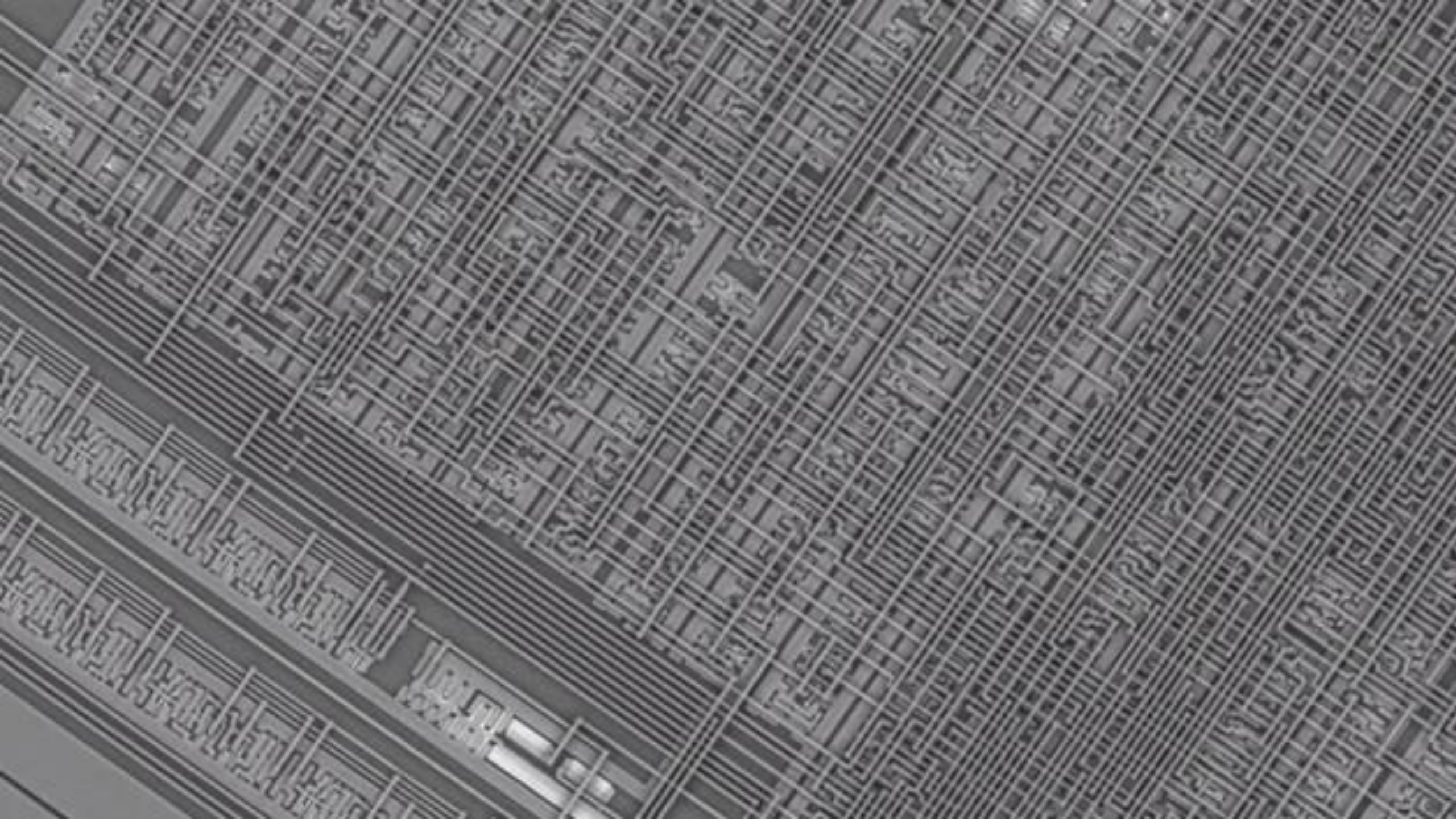


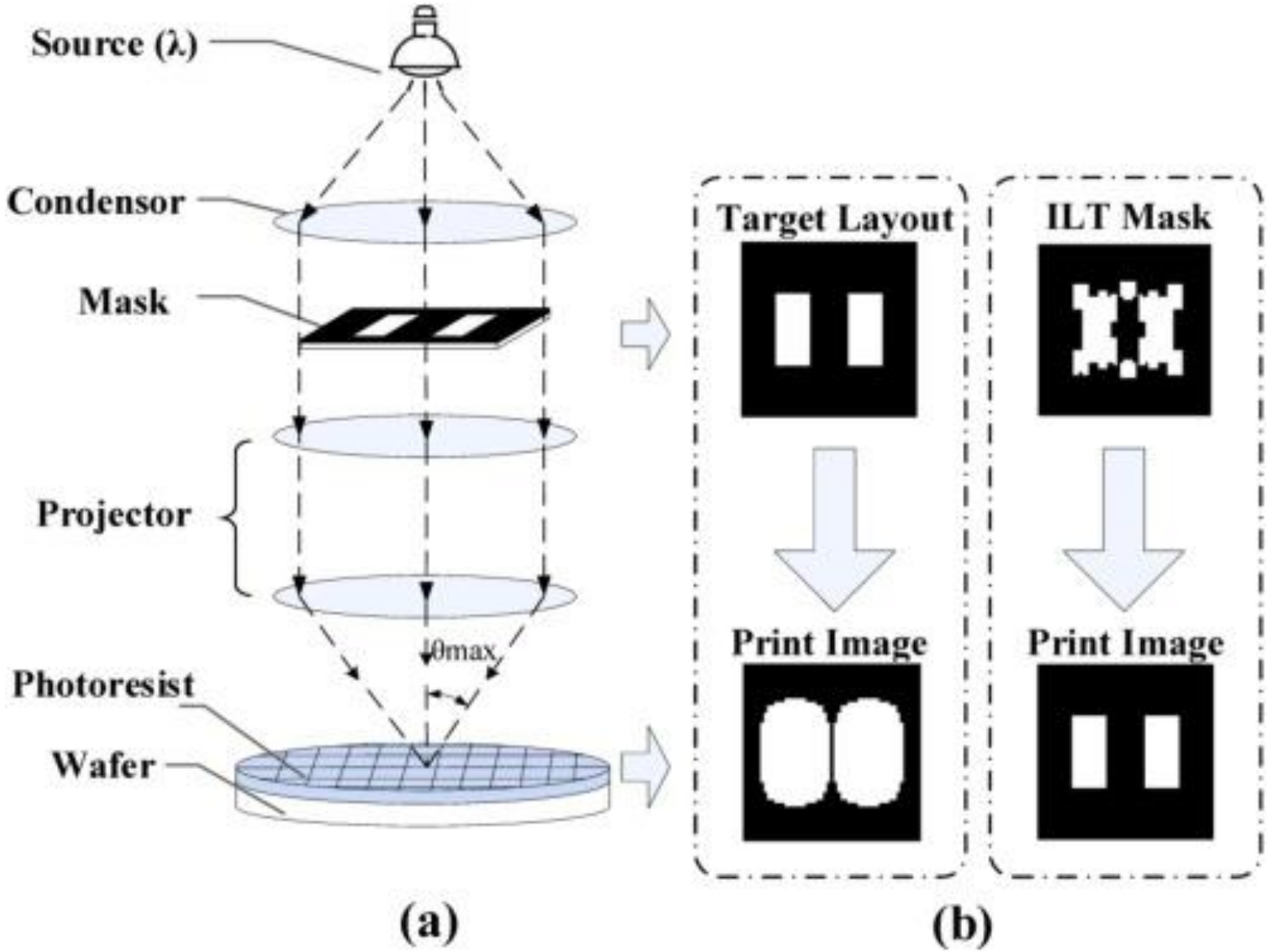
M1 Pro

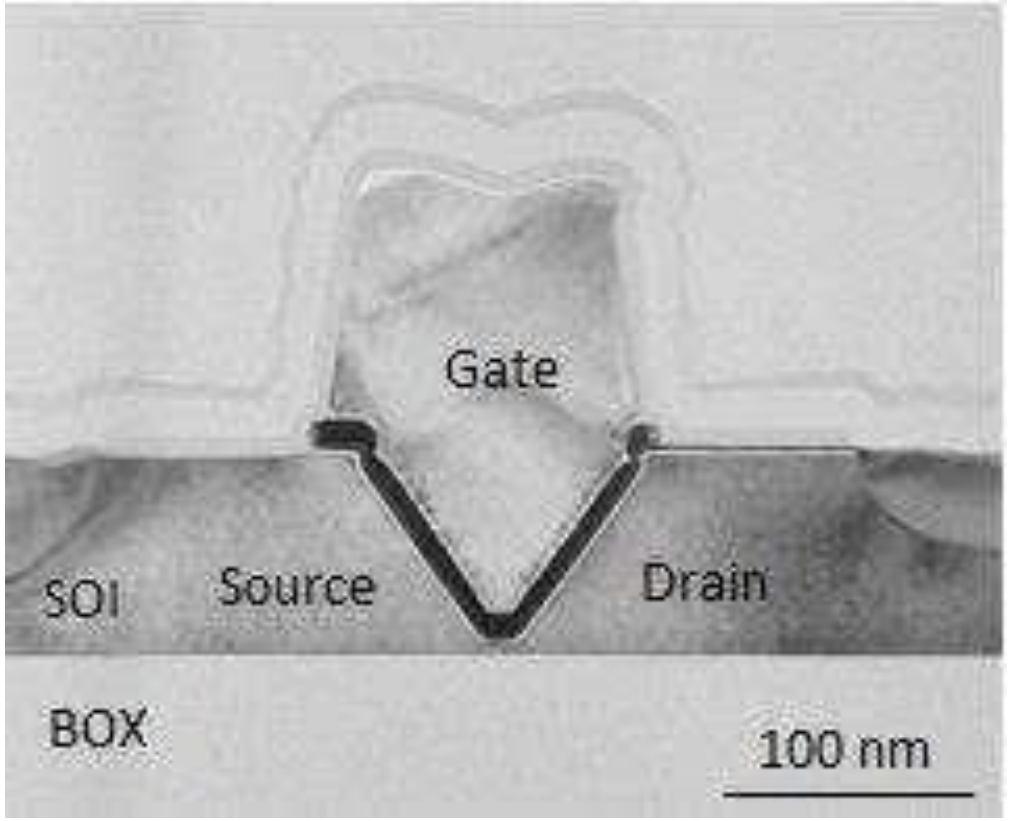


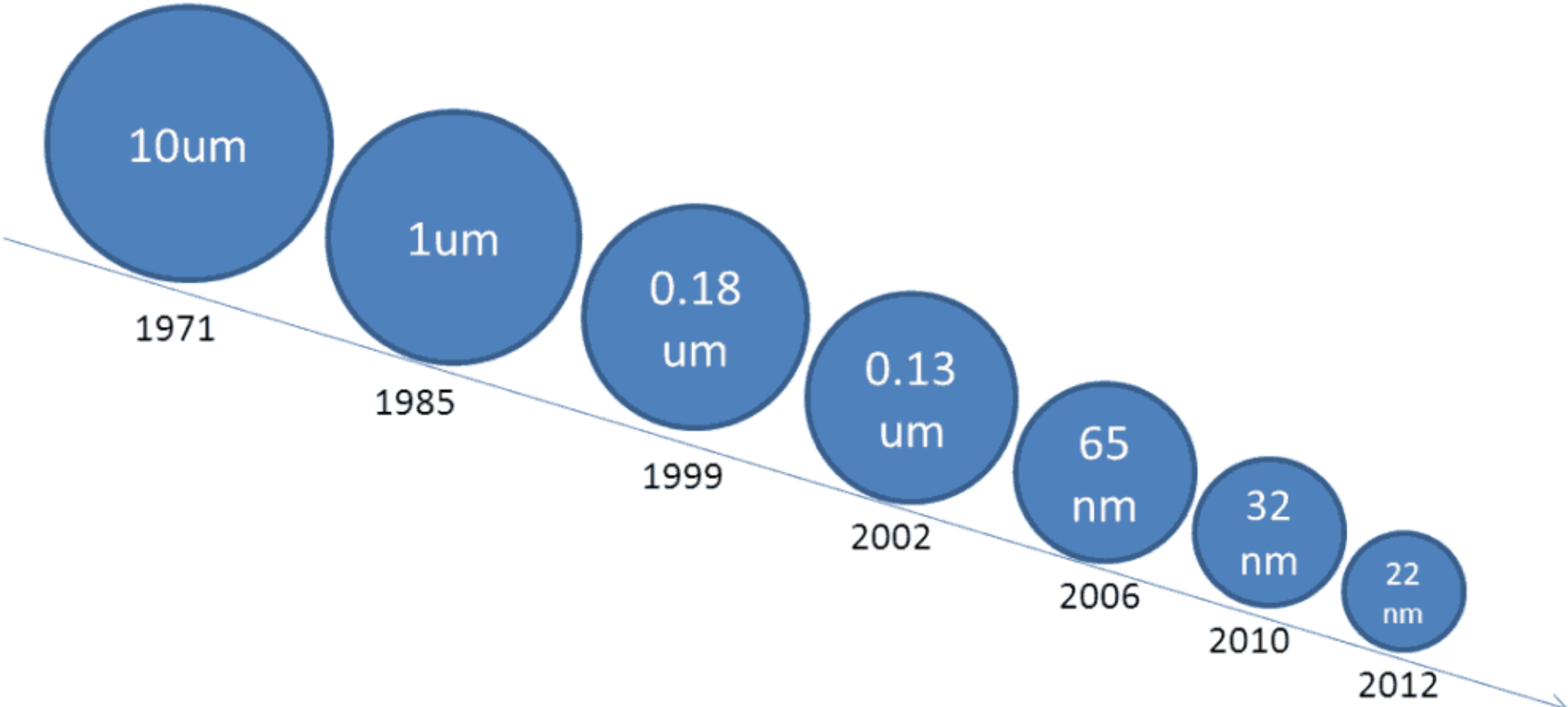
M1 Max

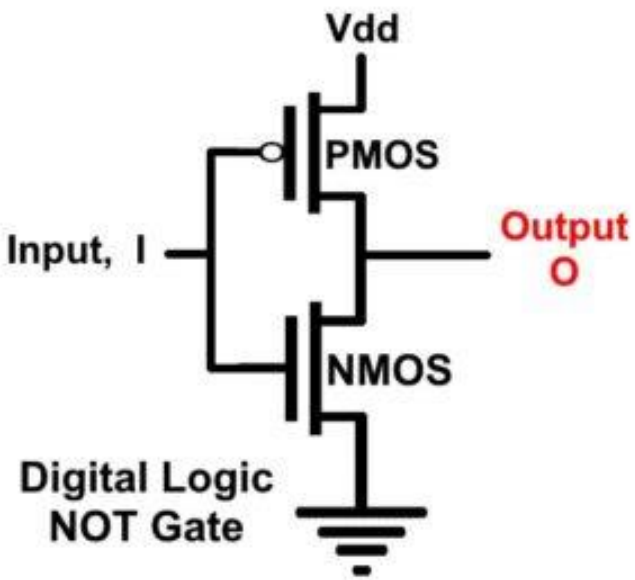


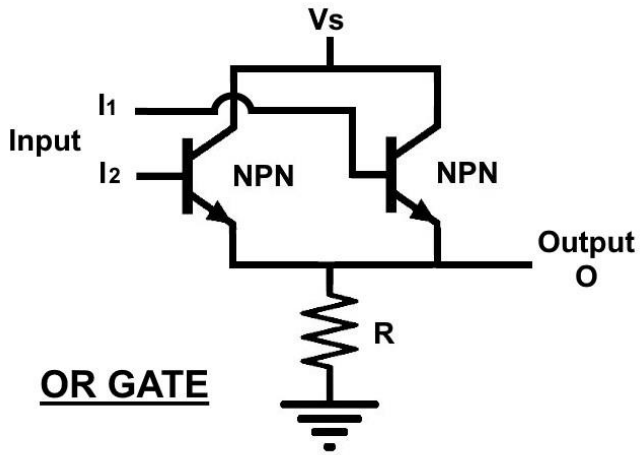


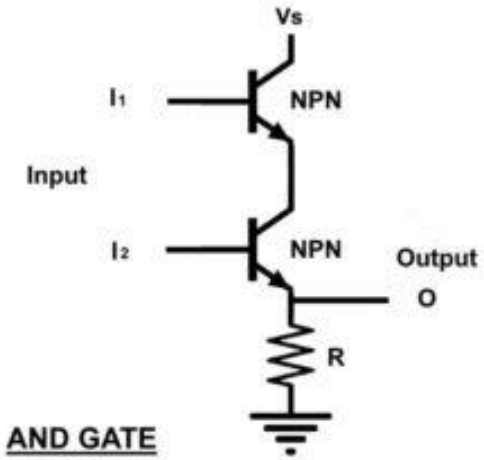

Source (λ)
Condensor
Mask
Projector
θmax
Photoresist
Wafer
Target Layout
ILT Mask
Print Image
Print Image
(a)
(b)

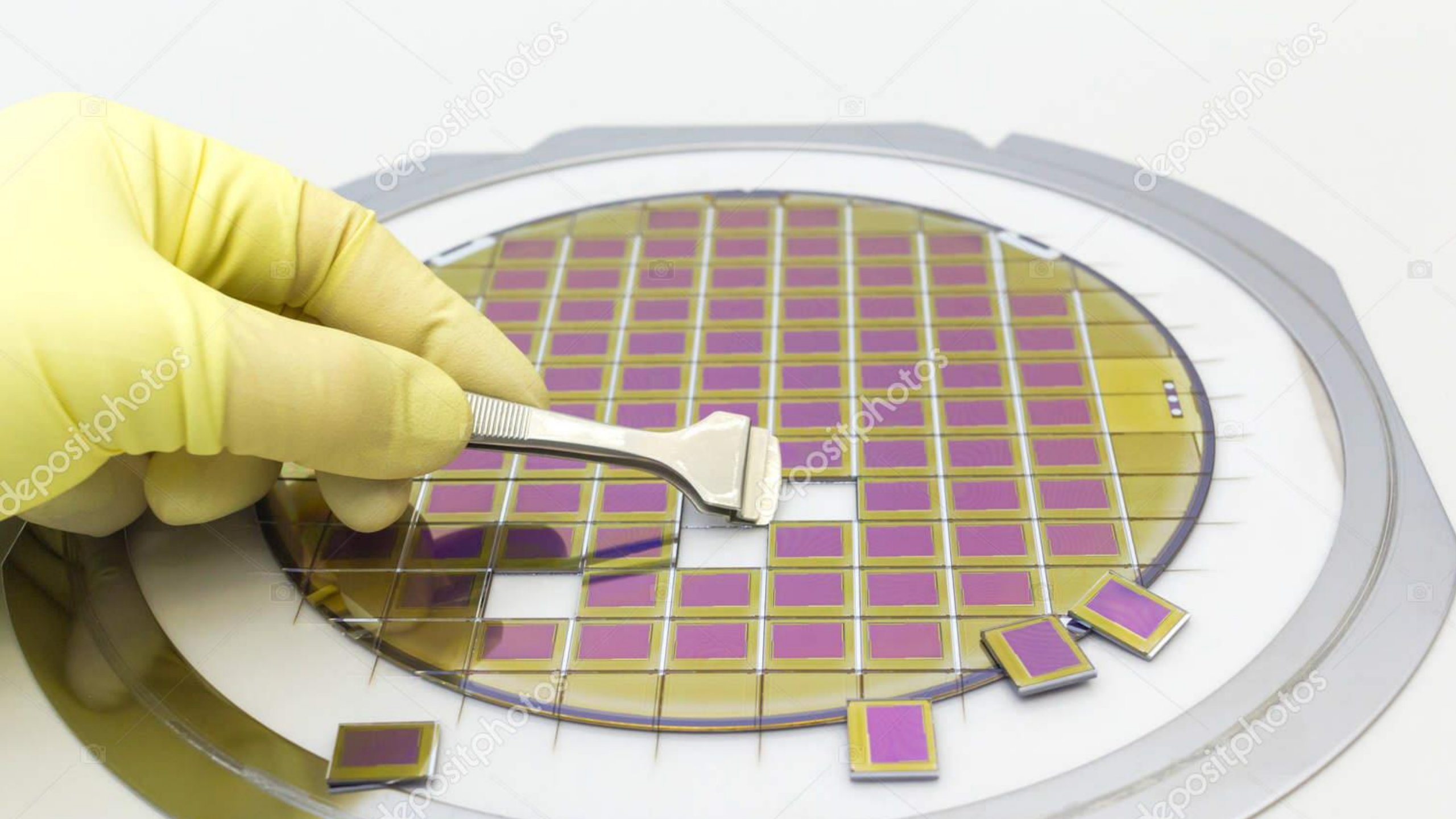

Gate
SOI
Source
Drain
BOX
100 nm

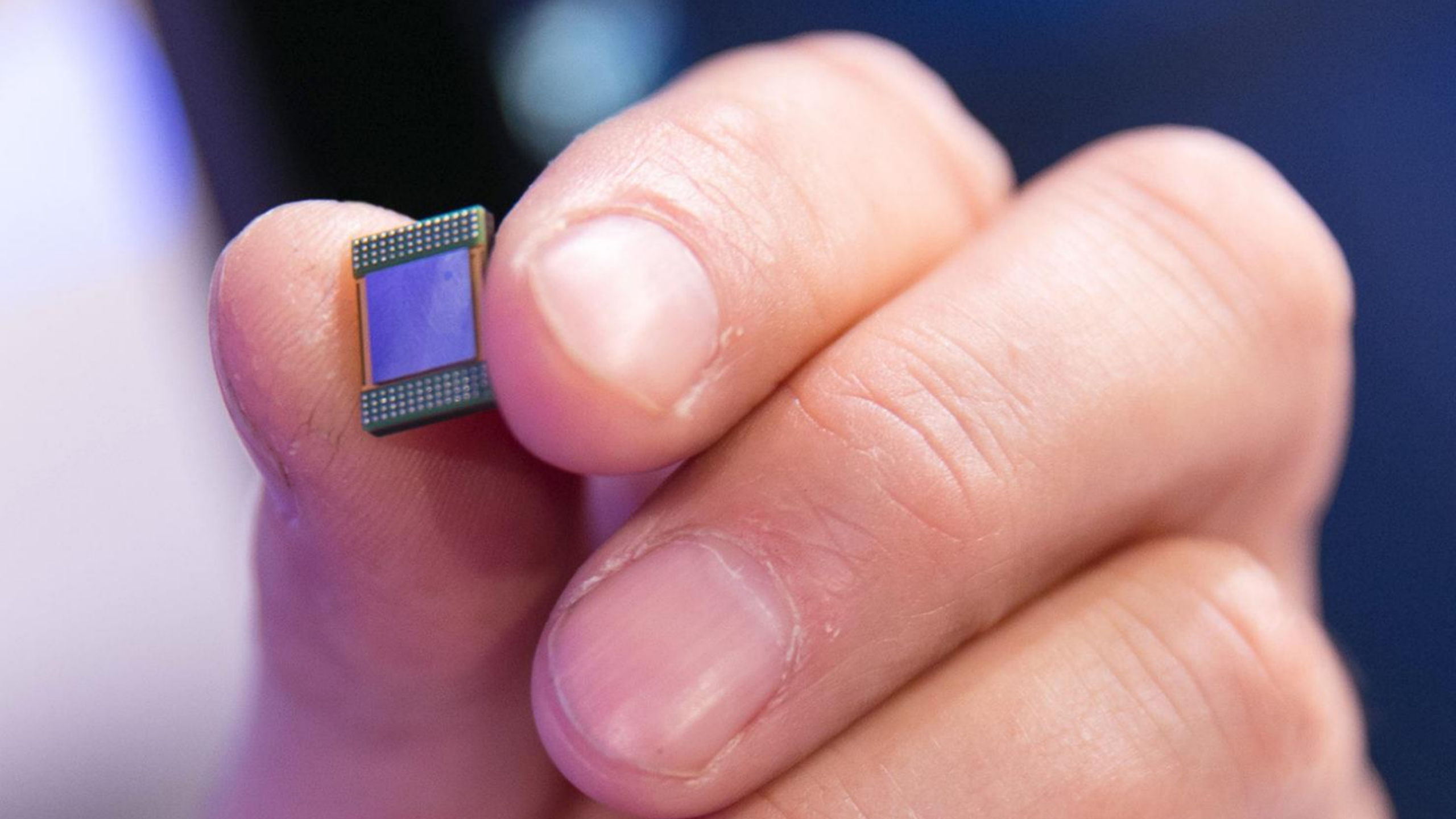

10um
1971
1um
1985
0.18 um
1999
0.13 um
2002
65 nm
2006
32 nm
2010
22 nm
2012

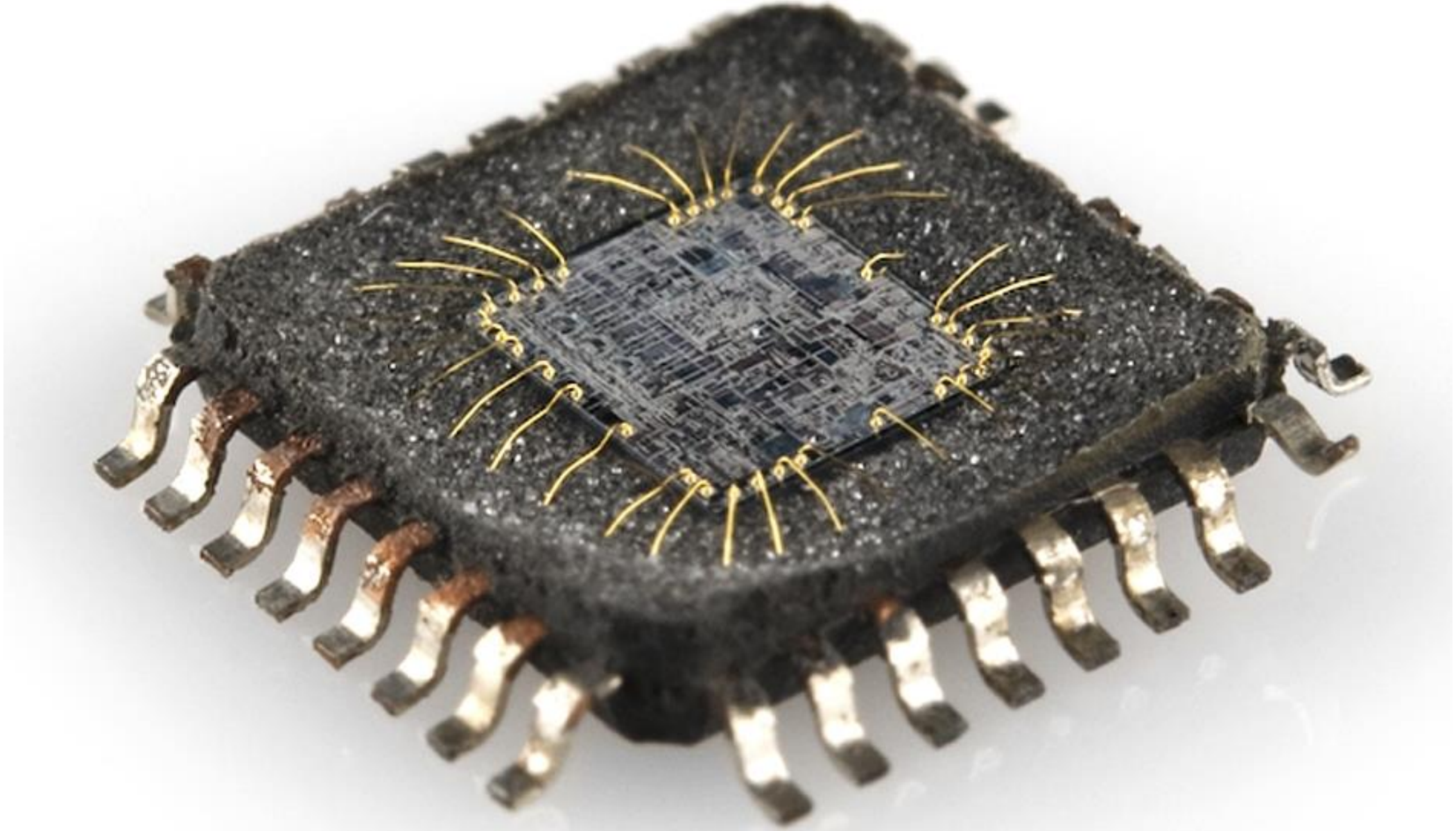

Vdd
PMOS
Input, I
Output
O
NMOS
Digital Logic
NOT Gate

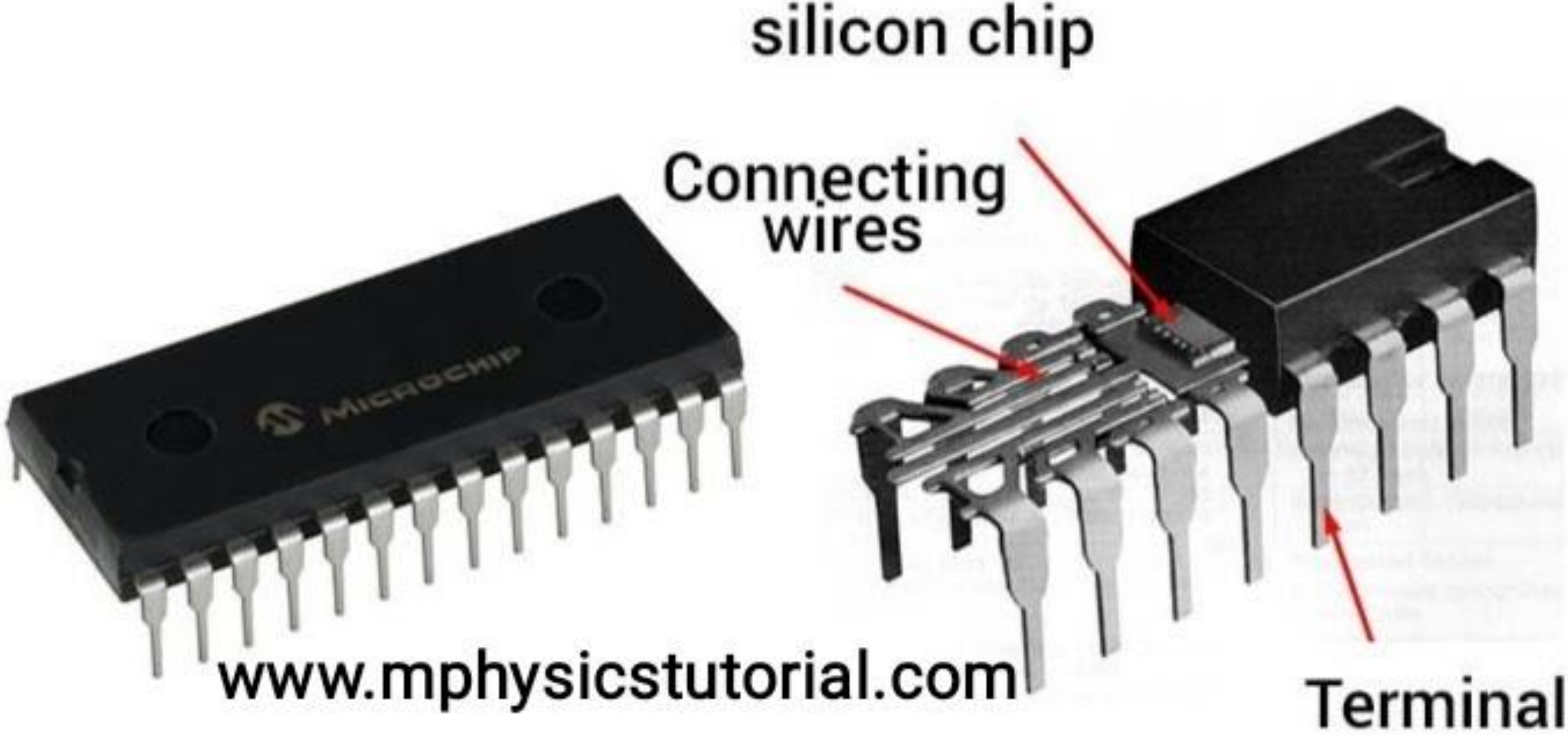

Vs
I1
Input
I2
NPN
NPN
Output
O
R
OR GATE

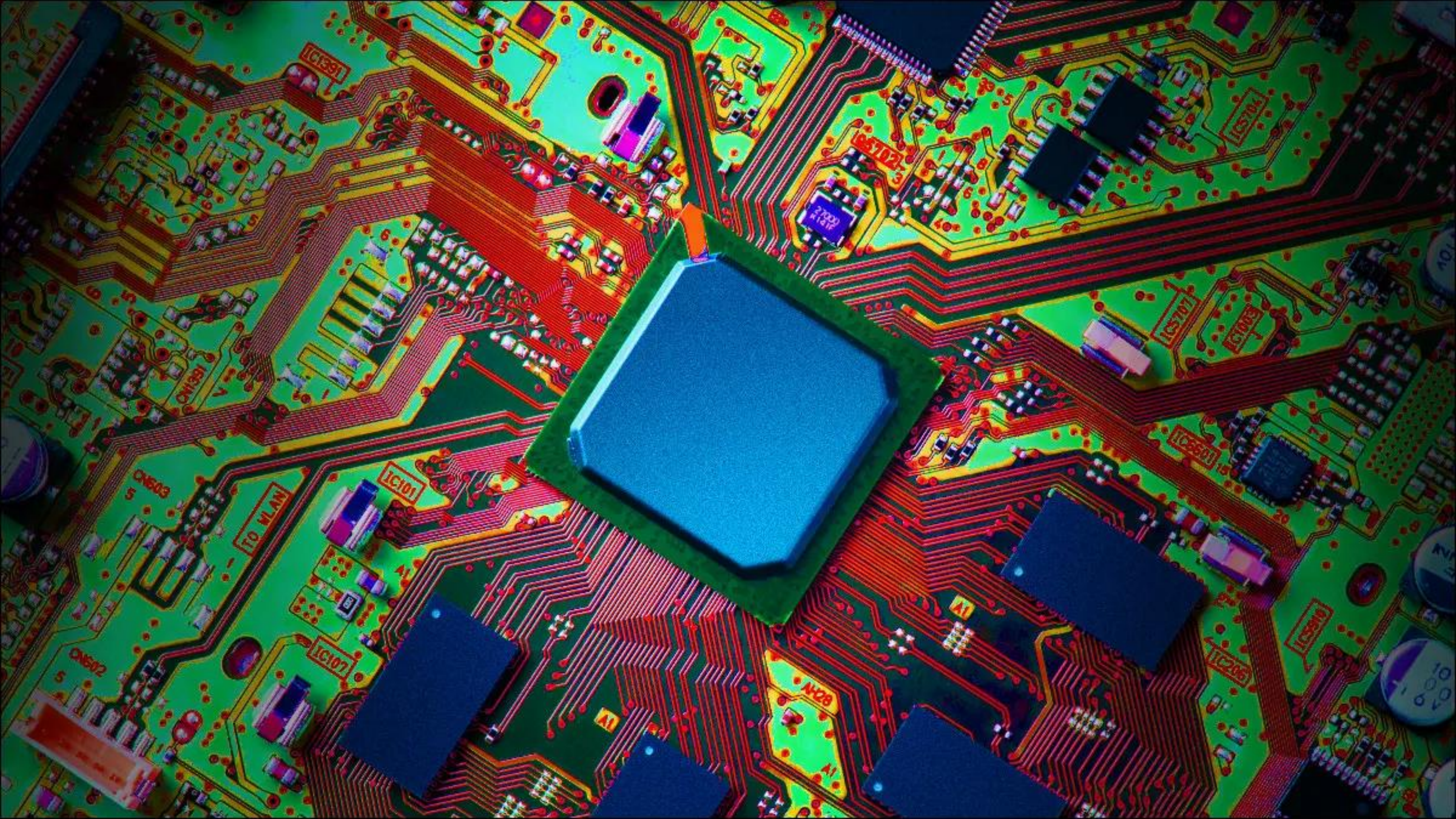

Vs
I1
NPN
Input
I2
NPN
Output
O
R
AND GATE





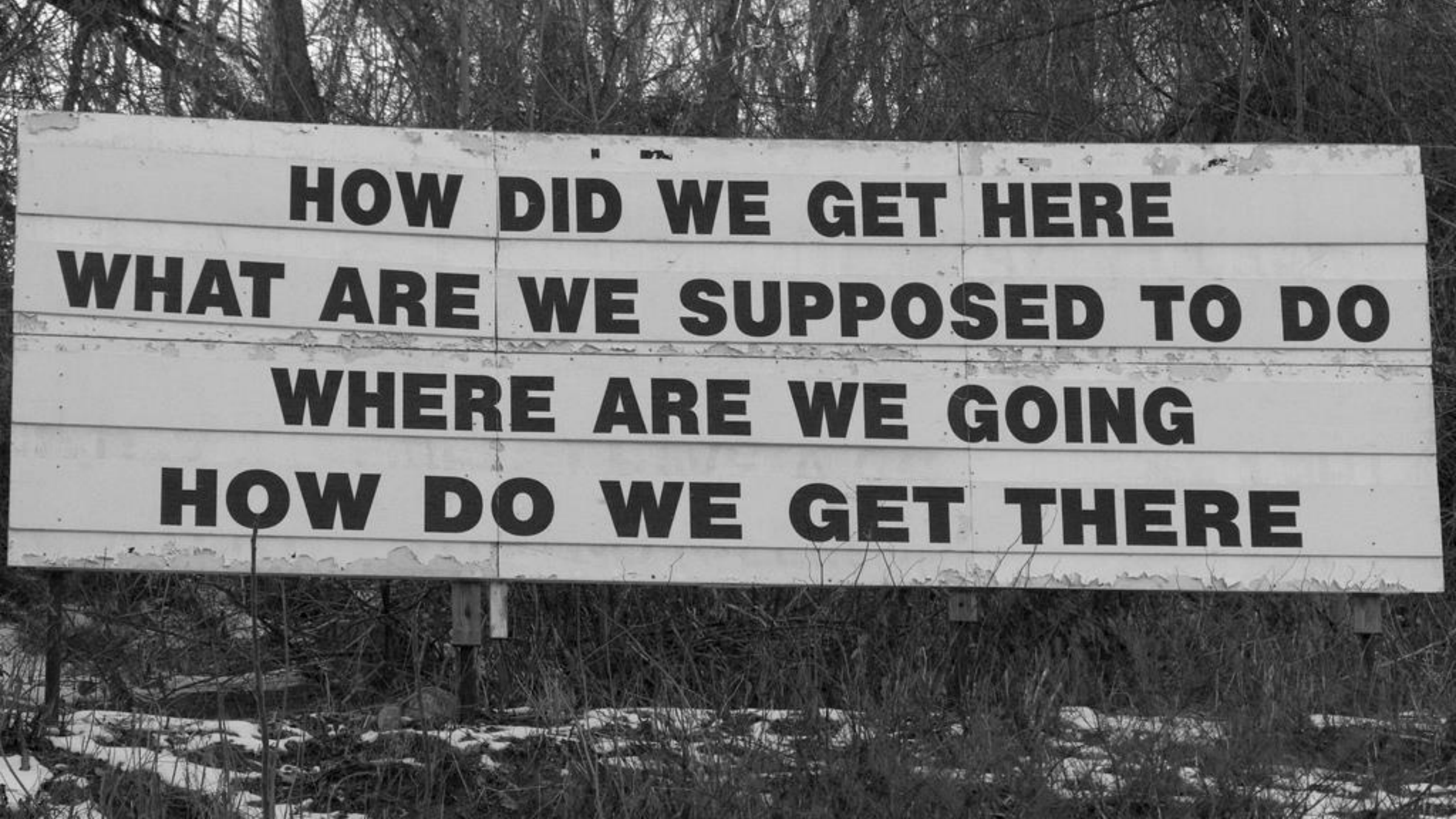


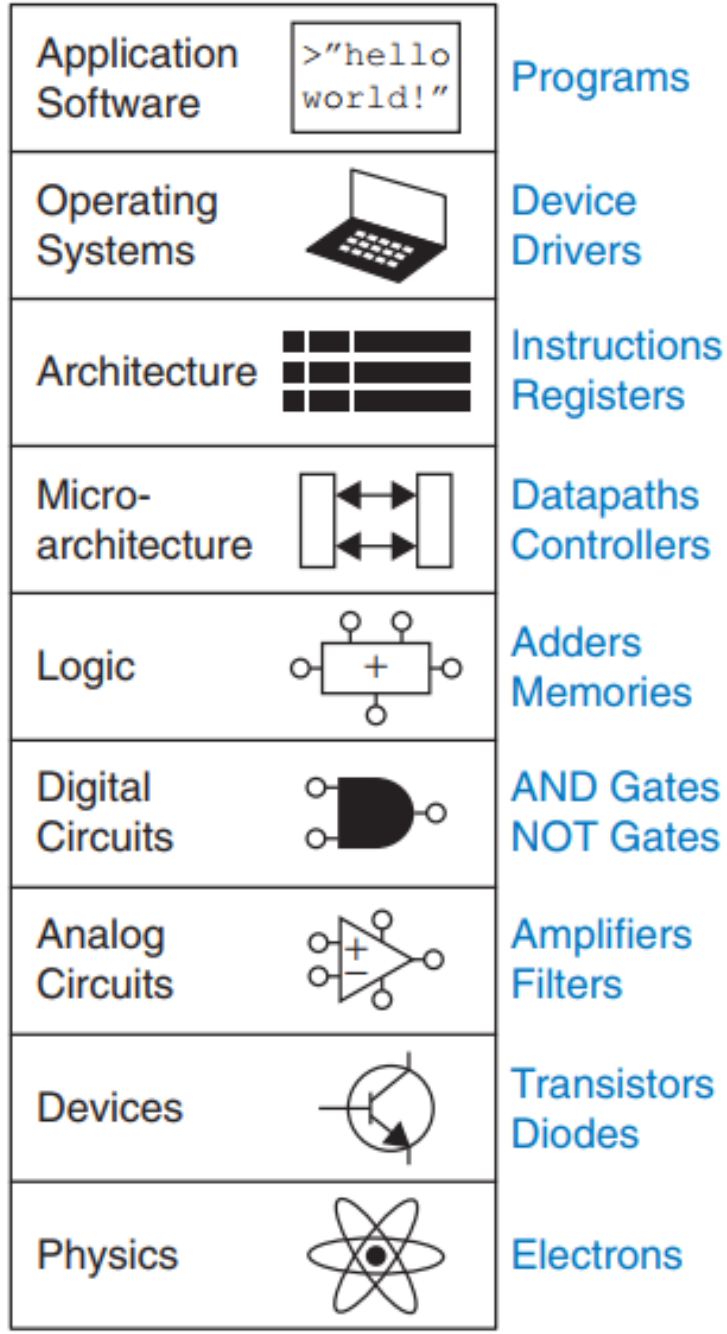

silicon chip
Connecting wires
MICROCHIP
www.mphysicstutorial.com
Terminal


TO WLAN
IC101
CN503
CN502

Grupitöö: Kuhu kiibid kadusid?

- Kuidas tekkis kiibikriis ja mida see tähendab?
- Kuidas saaks lahendada kriisi?
- **Miks on kriisi keskmes just kiibid?**


HOW DID WE GET HERE
WHAT ARE WE SUPPOSED TO DO
WHERE ARE WE GOING
HOW DO WE GET THERE

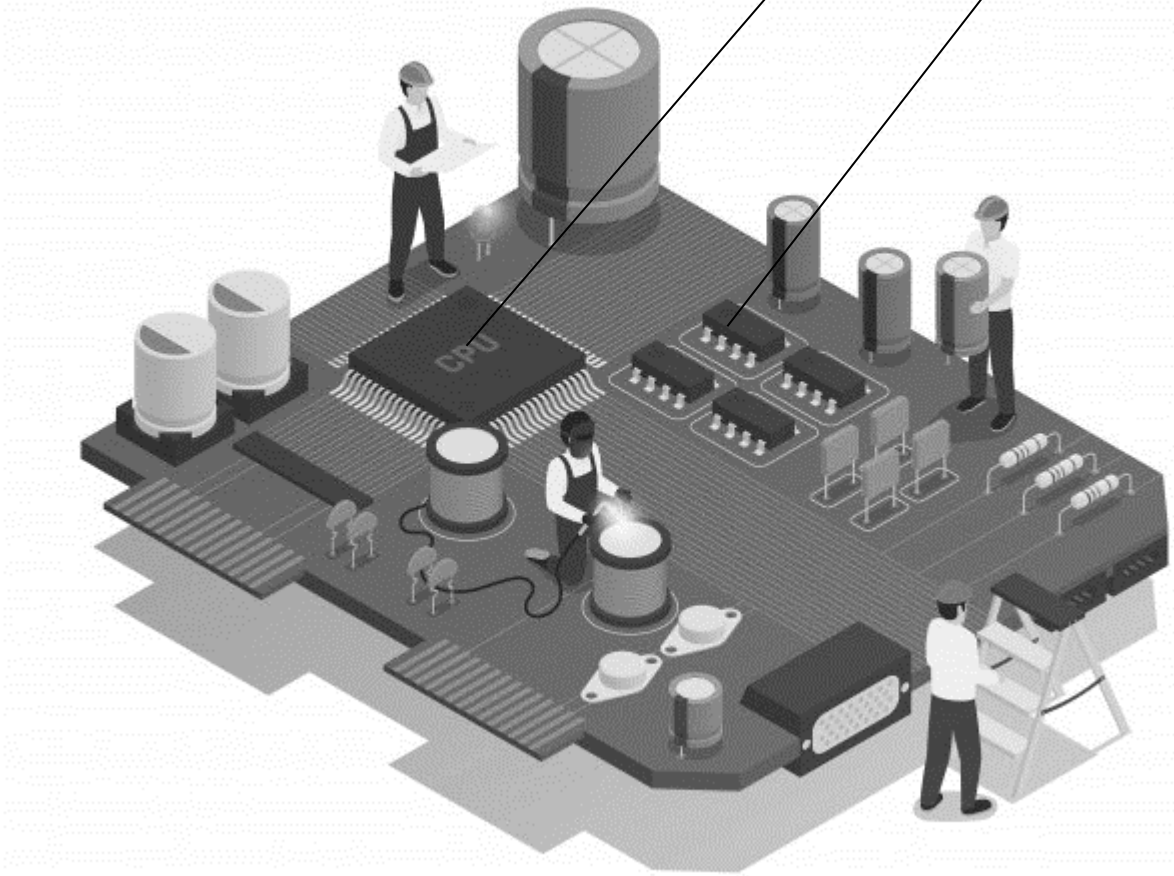


Nt. Office, Mail

Nt. Windows 10; OSX

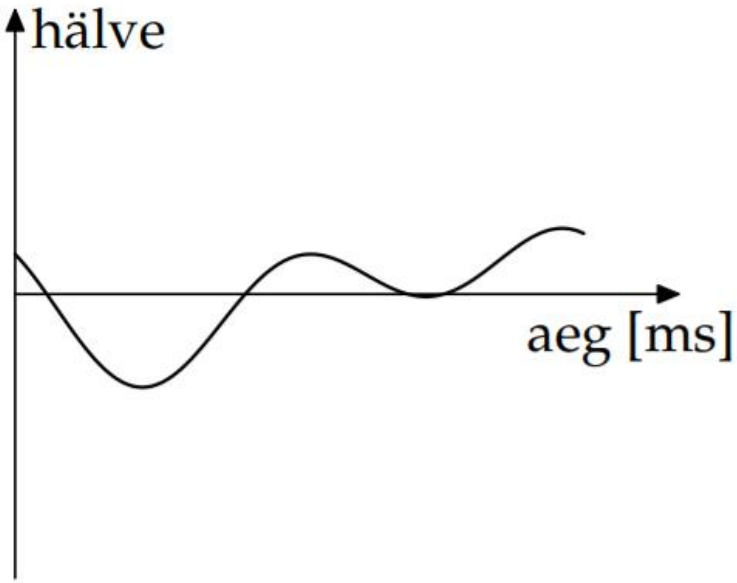
Nt. Inter x86; ARM

Nt. NetBurst; Nehalem



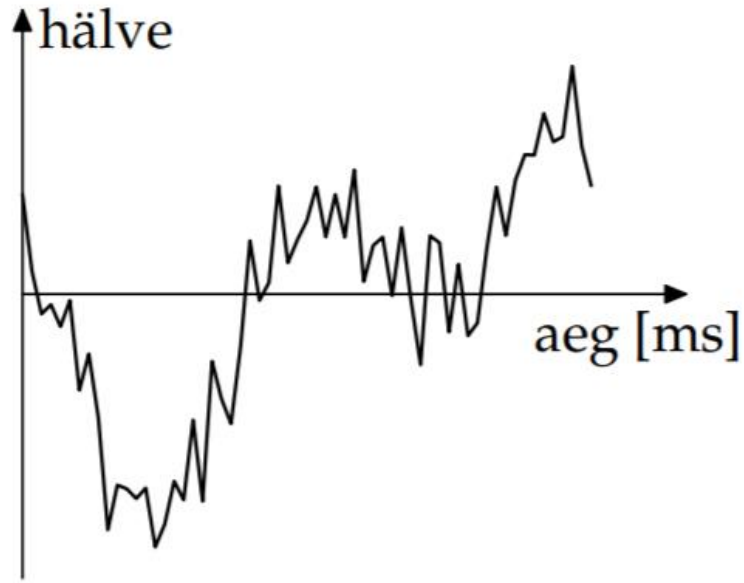
CPU (**central processing unit)**

PIC **microcontrollers**

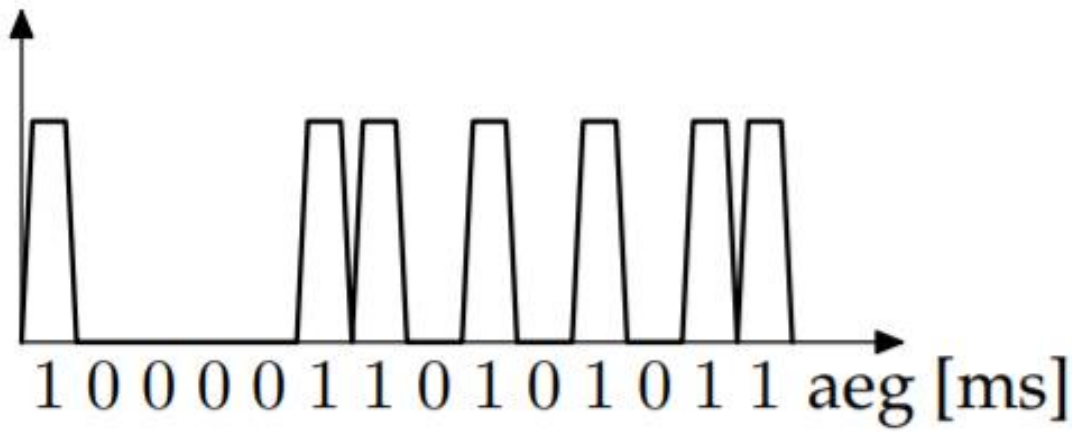


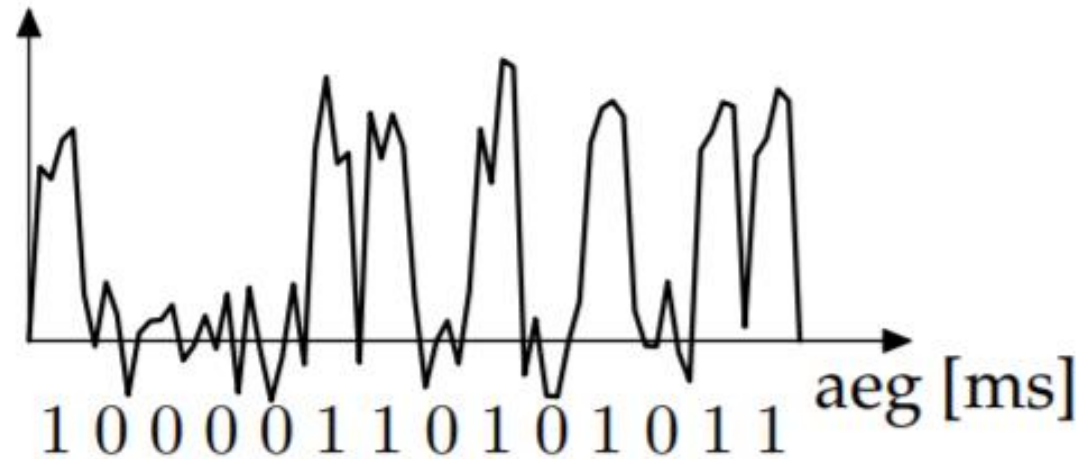
Joonis 2. Analoogsignaal mikrofonist

Joonis 3. Mürane analoogsignaal

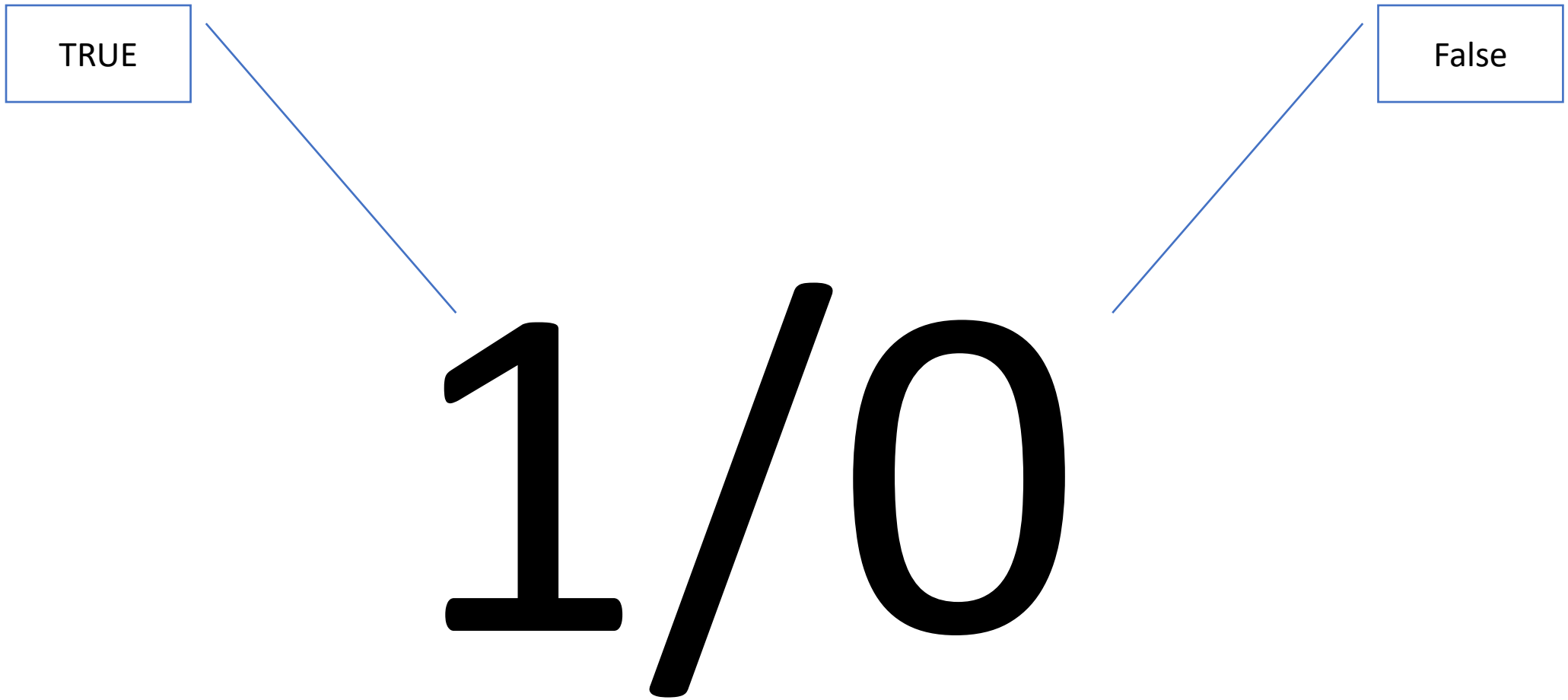


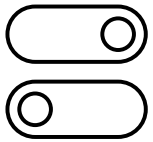
Joonis 4. Võimendatud mürane analoogsignaal


1 0 0 0 0 1 1 0 1 0 1 0 1 1 aeg [ms]


1 0 0 0 0 1 1 0 1 0 1 0 1 1
aeg [ms]

Analoogsignaal	**Digitaalsignaal**
Liinisisend (helikaardi Line In)	Paralleelport (LPT)
Liiniväljund (helikaardi Line Out)	Jadaport (COM)
Mikrofonsisend (helikaardi Mic In)	Jadaport (USB)
Videokaardi VGA-väljund	Videokaardi DVI-väljund
Komposiit-video	Game-port
S-video	Võrgukaardi ühendused (keerupaar, koaksiaal)
Komponent-video (RCA)	
SCART	
Telefoniliin	

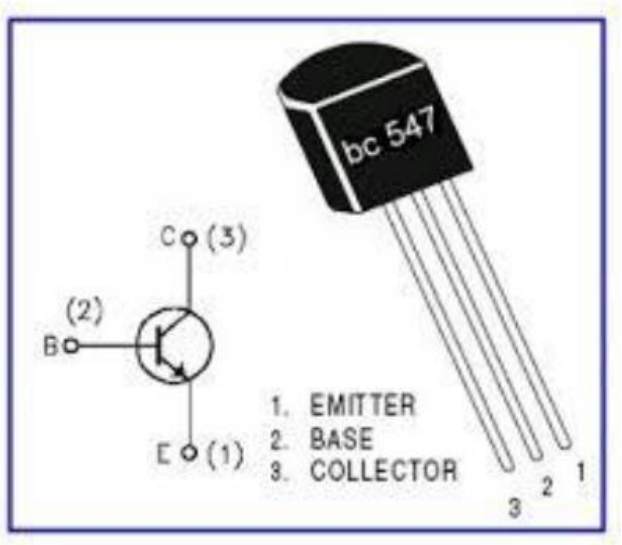

TRUE
False
1/0



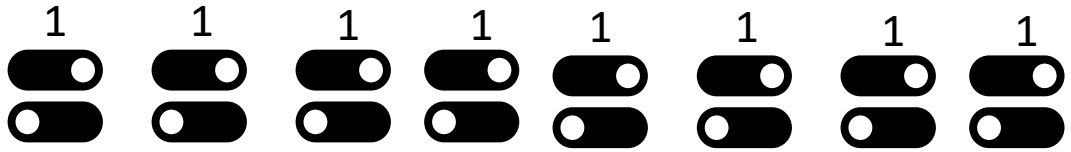
Off = 0 (0 V/DC)

ON = 1 (+5 v/DC)

0-4mA; 1-20mA;
0-0.5V;
1-2.4 V
3.3V
5 V



1958.a.



8 x 1 bit = 1 Byte

Decimal	Binary
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

1963. aastal loodi keel ASCII – Ameerika Standard kood

ASCII TABLE

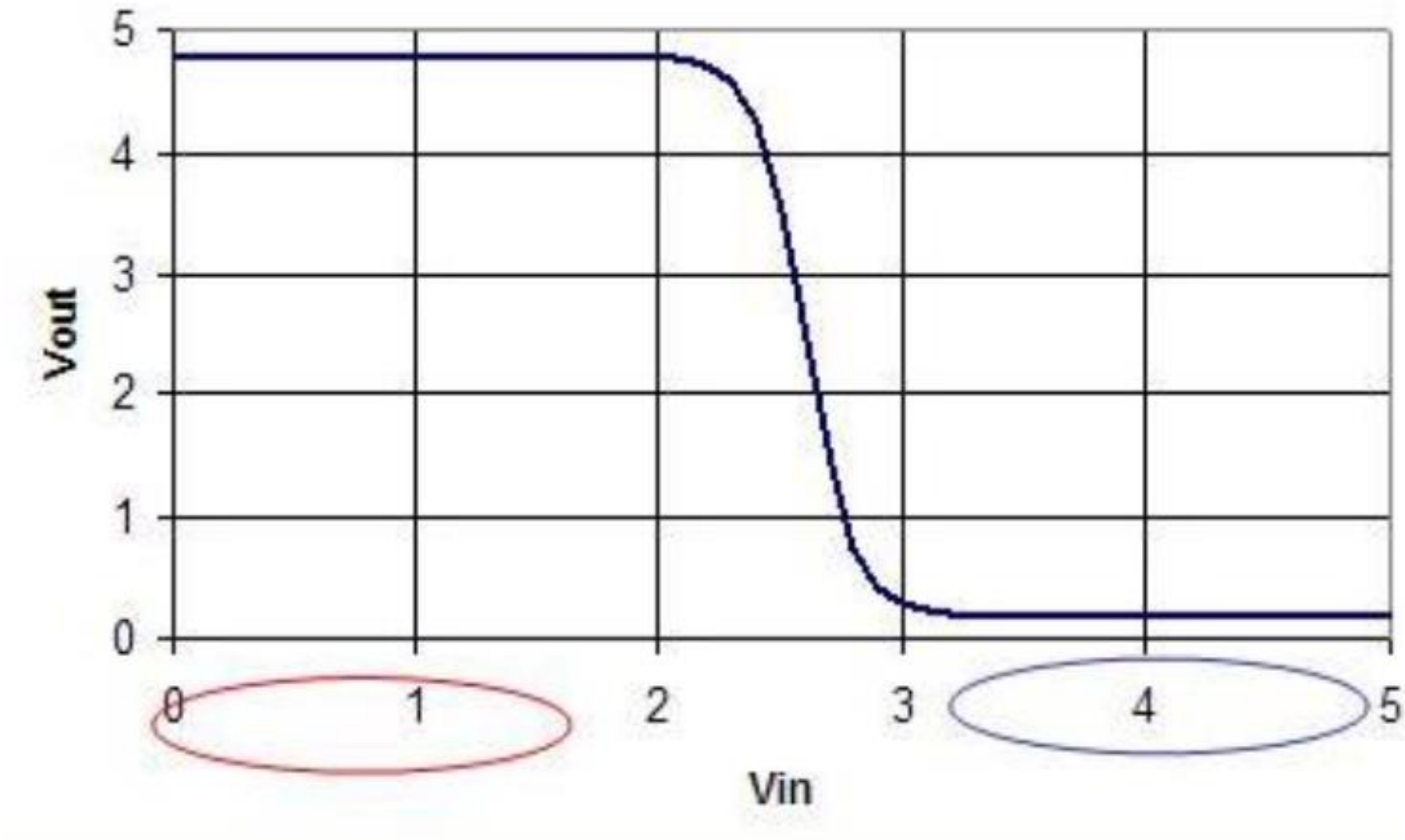
Decimal	Hexadecimal	Binary	Octal	Char
0	0	0	0	*[NULL]*
1	1	1	1	*[START OF HEADING]*
2	2	10	2	*[START OF TEXT]*
3	3	11	3	*[END OF TEXT]*
4	4	100	4	*[END OF TRANSMISSION]*
5	5	101	5	*[ENQUIRY]*
6	6	110	6	*[ACKNOWLEDGE]*
7	7	111	7	*[BELL]*
8	8	1000	10	*[BACKSPACE]*
9	9	1001	11	*[HORIZONTAL TAB]*
10	A	1010	12	*[LINE FEED]*
11	B	1011	13	*[VERTICAL TAB]*
12	C	1100	14	*[FORM FEED]*
13	D	1101	15	*[CARRIAGE RETURN]*
14	E	1110	16	*[SHIFT OUT]*
15	F	1111	17	*[SHIFT IN]*
16	10	10000	20	*[DATA LINK ESCAPE]*
17	11	10001	21	*[DEVICE CONTROL 1]*
18	12	10010	22	*[DEVICE CONTROL 2]*
19	13	10011	23	*[DEVICE CONTROL 3]*
20	14	10100	24	*[DEVICE CONTROL 4]*
21	15	10101	25	*[NEGATIVE ACKNOWLEDGE]*
22	16	10110	26	*[SYNCHRONOUS IDLE]*
23	17	10111	27	*[ENG OF TRANS. BLOCK]*
24	18	11000	30	*[CANCEL]*
25	19	11001	31	*[END OF MEDIUM]*
26	1A	11010	32	*[SUBSTITUTE]*
27	1B	11011	33	*[ESCAPE]*
28	1C	11100	34	*[FILE SEPARATOR]*
29	1D	11101	35	*[GROUP SEPARATOR]*
30	1E	11110	36	*[RECORD SEPARATOR]*
31	1F	11111	37	*[UNIT SEPARATOR]*
32	20	100000	40	*[SPACE]*
33	21	100001	41	!
34	22	100010	42	"
35	23	100011	43	#
36	24	100100	44	$
37	25	100101	45	%
38	26	100110	46	&
39	27	100111	47	'
40	28	101000	50	(
41	29	101001	51	)
42	2A	101010	52	*
43	2B	101011	53	+
44	2C	101100	54	,
45	2D	101101	55	-
46	2E	101110	56	.
47	2F	101111	57	/
48	30	110000	60	**0**
49	31	110001	61	**1**
50	32	110010	62	**2**
51	33	110011	63	**3**
52	34	110100	64	**4**
53	35	110101	65	**5**
54	36	110110	66	**6**
55	37	110111	67	**7**
56	38	111000	70	**8**
57	39	111001	71	**9**
58	3A	111010	72	:
59	3B	111011	73	;
60	3C	111100	74	<
61	3D	111101	75	=
62	3E	111110	76	>
63	3F	111111	77	?
64	40	1000000	100	@
65	41	1000001	101	**A**
66	42	1000010	102	**B**
67	43	1000011	103	**C**
68	44	1000100	104	**D**
69	45	1000101	105	**E**
70	46	1000110	106	**F**
71	47	1000111	107	**G**
72	48	1001000	110	**H**
73	49	1001001	111	**I**
74	4A	1001010	112	**J**
75	4B	1001011	113	**K**
76	4C	1001100	114	**L**
77	4D	1001101	115	**M**
78	4E	1001110	116	**N**
79	4F	1001111	117	**O**
80	50	1010000	120	**P**
81	51	1010001	121	**Q**
82	52	1010010	122	**R**
83	53	1010011	123	**S**
84	54	1010100	124	**T**
85	55	1010101	125	**U**
86	56	1010110	126	**V**
87	57	1010111	127	**W**
88	58	1011000	130	**X**
89	59	1011001	131	**Y**
90	5A	1011010	132	**Z**
91	5B	1011011	133	**[**
92	5C	1011100	134	\
93	5D	1011101	135	**]**
94	5E	1011110	136	^
95	5F	1011111	137	_
96	60	1100000	140	`
97	61	1100001	141	**a**
98	62	1100010	142	**b**
99	63	1100011	143	**c**
100	64	1100100	144	**d**
101	65	1100101	145	**e**
102	66	1100110	146	**f**
103	67	1100111	147	**g**
104	68	1101000	150	**h**
105	69	1101001	151	**i**
106	6A	1101010	152	**j**
107	6B	1101011	153	**k**
108	6C	1101100	154	**l**
109	6D	1101101	155	**m**
110	6E	1101110	156	**n**
111	6F	1101111	157	**o**
112	70	1110000	160	**p**
113	71	1110001	161	**q**
114	72	1110010	162	**r**
115	73	1110011	163	**s**
116	74	1110100	164	**t**
117	75	1110101	165	**u**
118	76	1110110	166	**v**
119	77	1110111	167	**w**
120	78	1111000	170	**x**
121	79	1111001	171	**y**
122	7A	1111010	172	**z**
123	7B	1111011	173	**{**
124	7C	1111100	174	**|**
125	7D	1111101	175	**}**
126	7E	1111110	176	~
127	7F	1111111	177	*[DEL]*

1982.a.

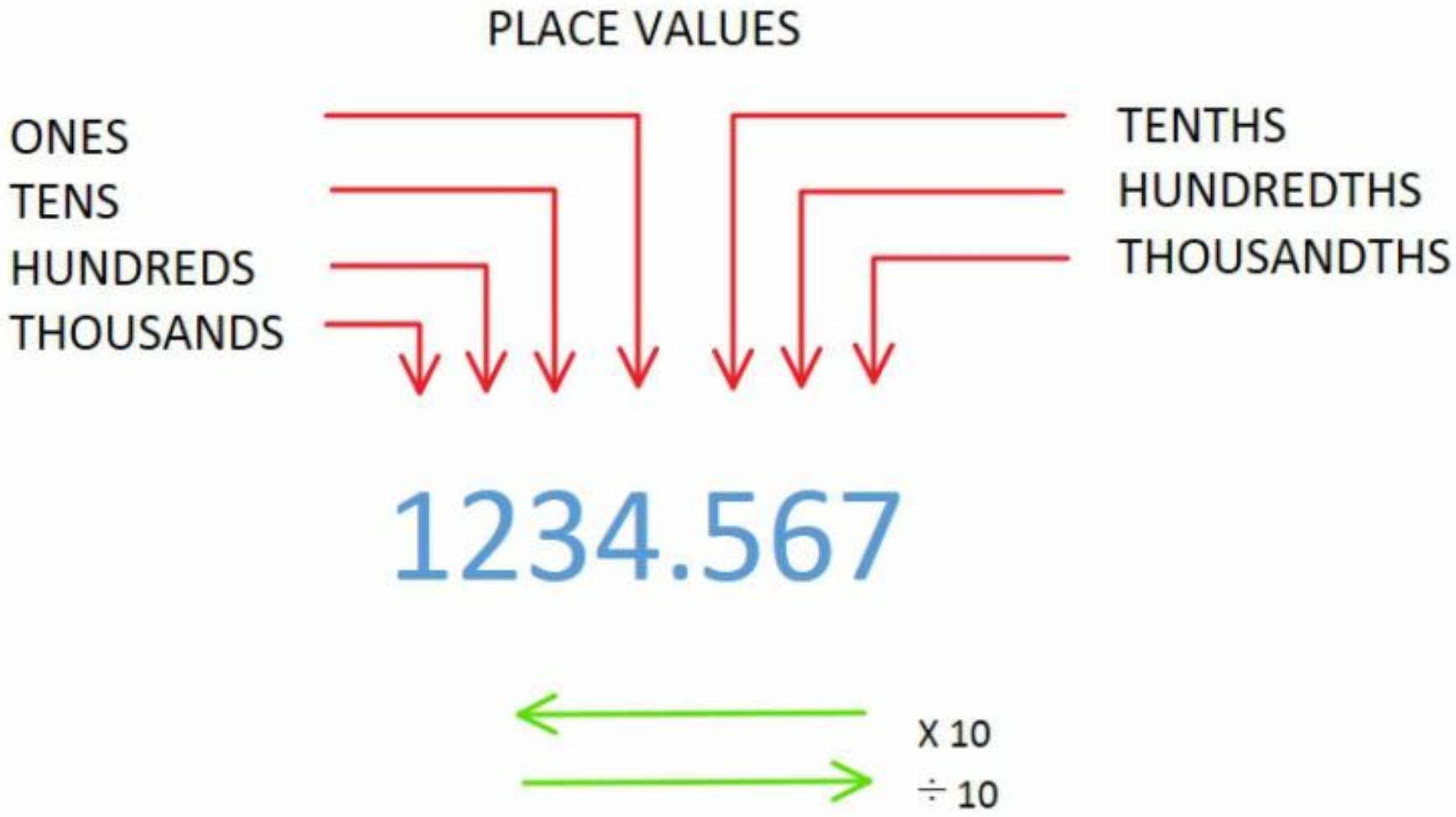
Sisend

Tehted

Väljund



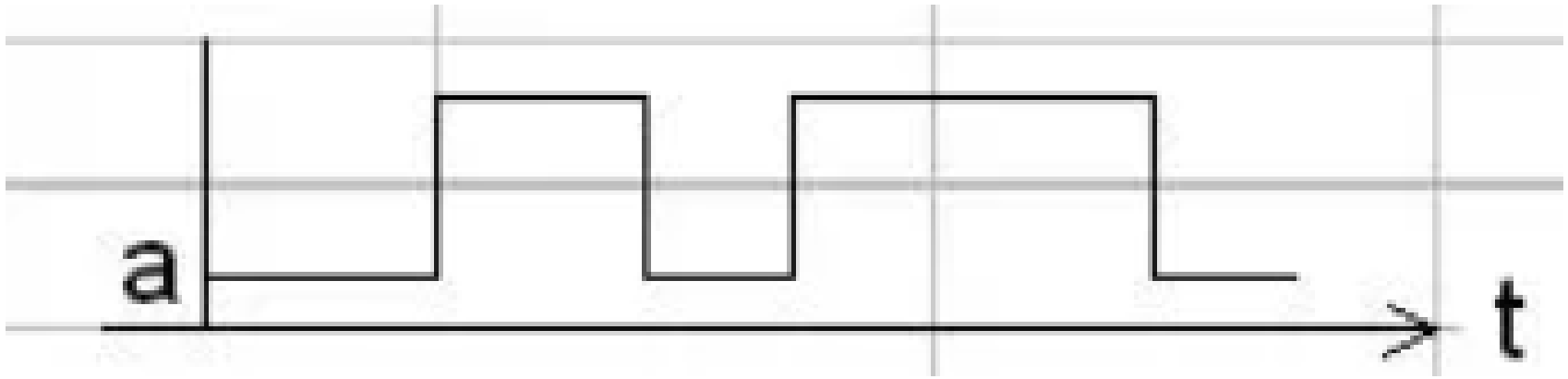
Oluline on, et signaale töötlevad komponendid „kinnitaks“ olekut ehk viiks muutuja võimalikult kindlalt ja kiiresti vajalikku olekusse

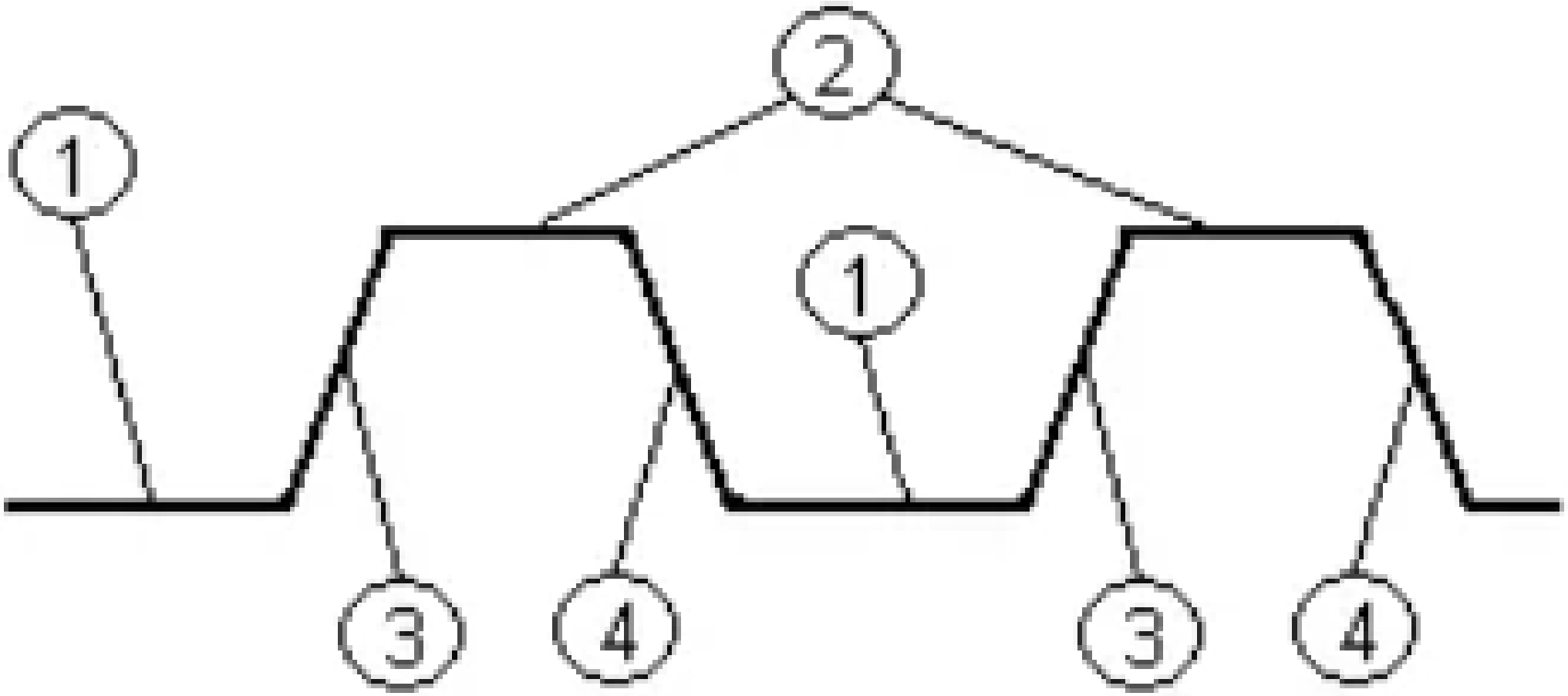


Decimal system

Sinaal – info edastamise viis

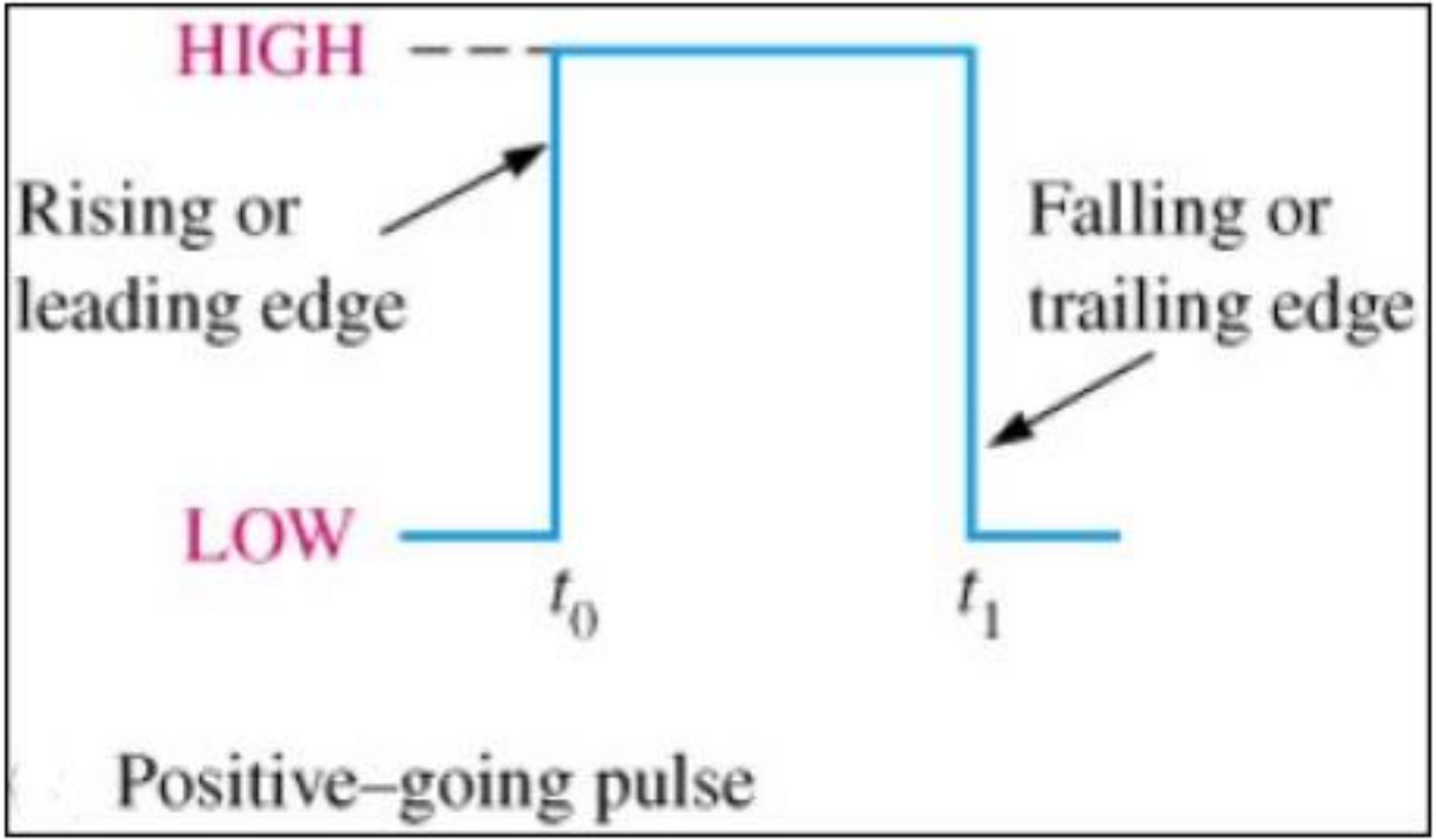
Diskreetne digitaalne signaal



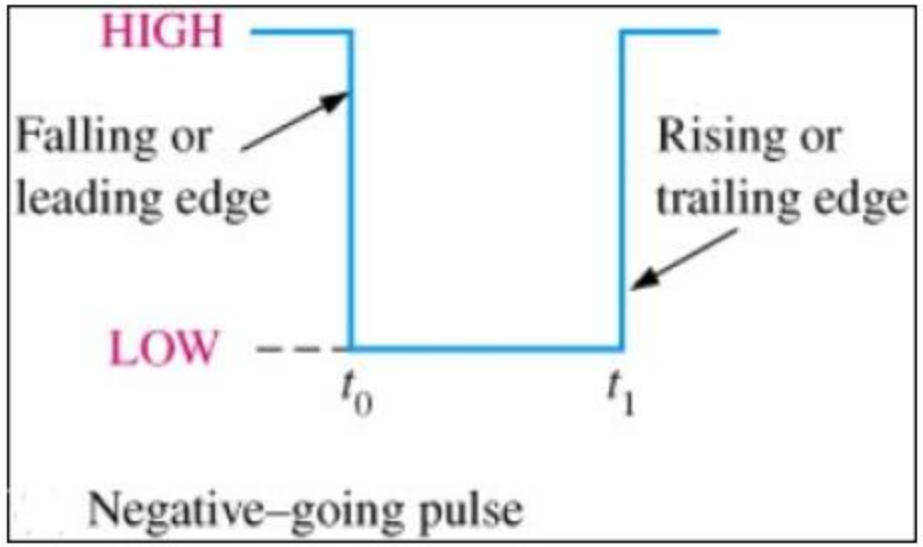


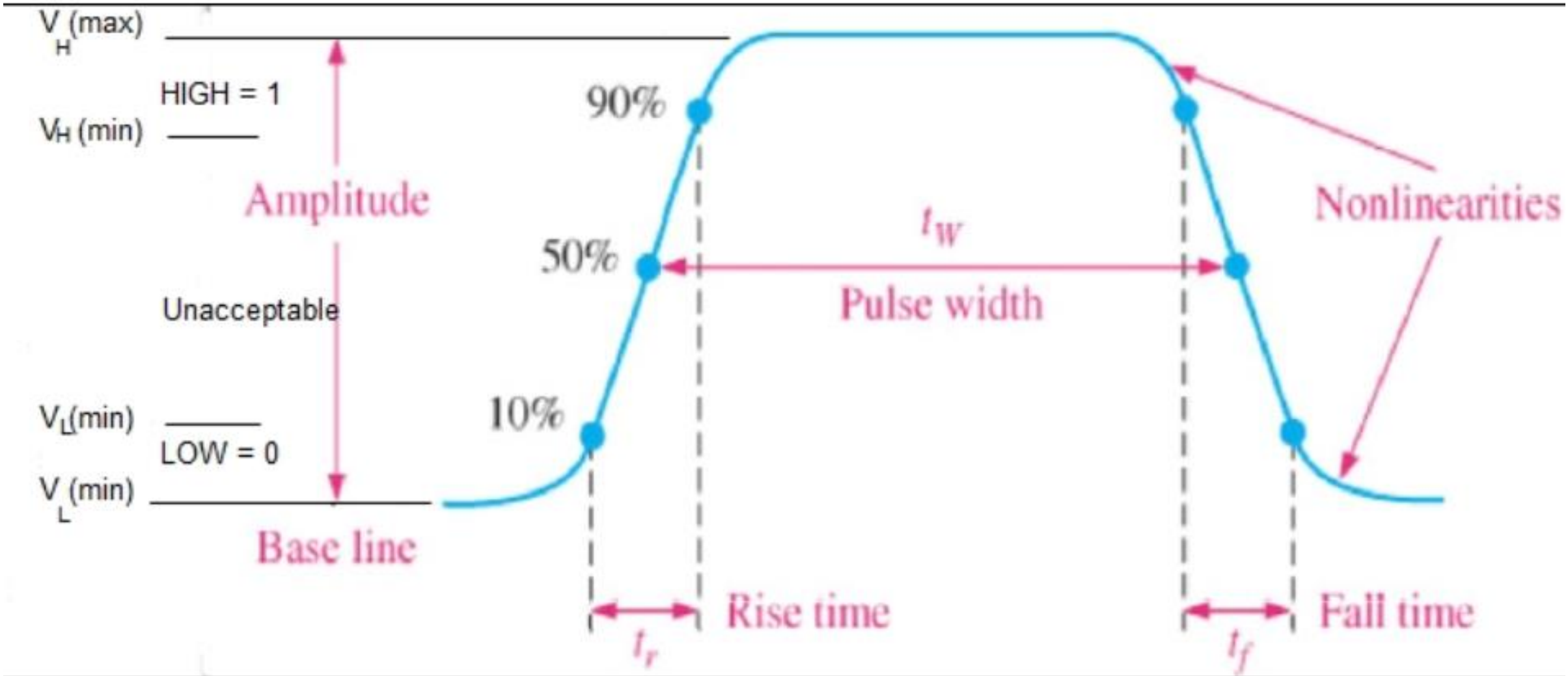
1 - madal signaalitase,
2 - kõrge signaalitase,
3 - signaali tõus (ees),
4 - signaali langus (piiriületus)

Positiivne impulss.

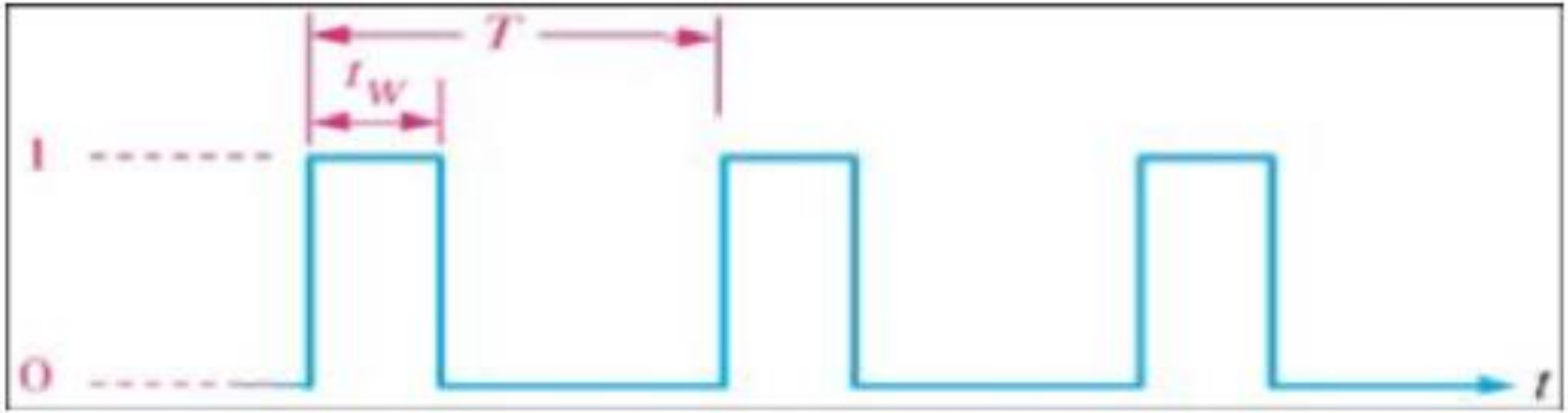


Negatiivne impulss.




V H (max)
HIGH = 1
V H (min)
Amplitude
Unacceptable
V L (min)
LOW = 0
V L (min)
Base line
90%
50%
10%
t_W
Pulse width
Nonlinearities
Rise time
t_r
Fall time
t_f

Käidutsükli näide.= tsüklit/sekundis



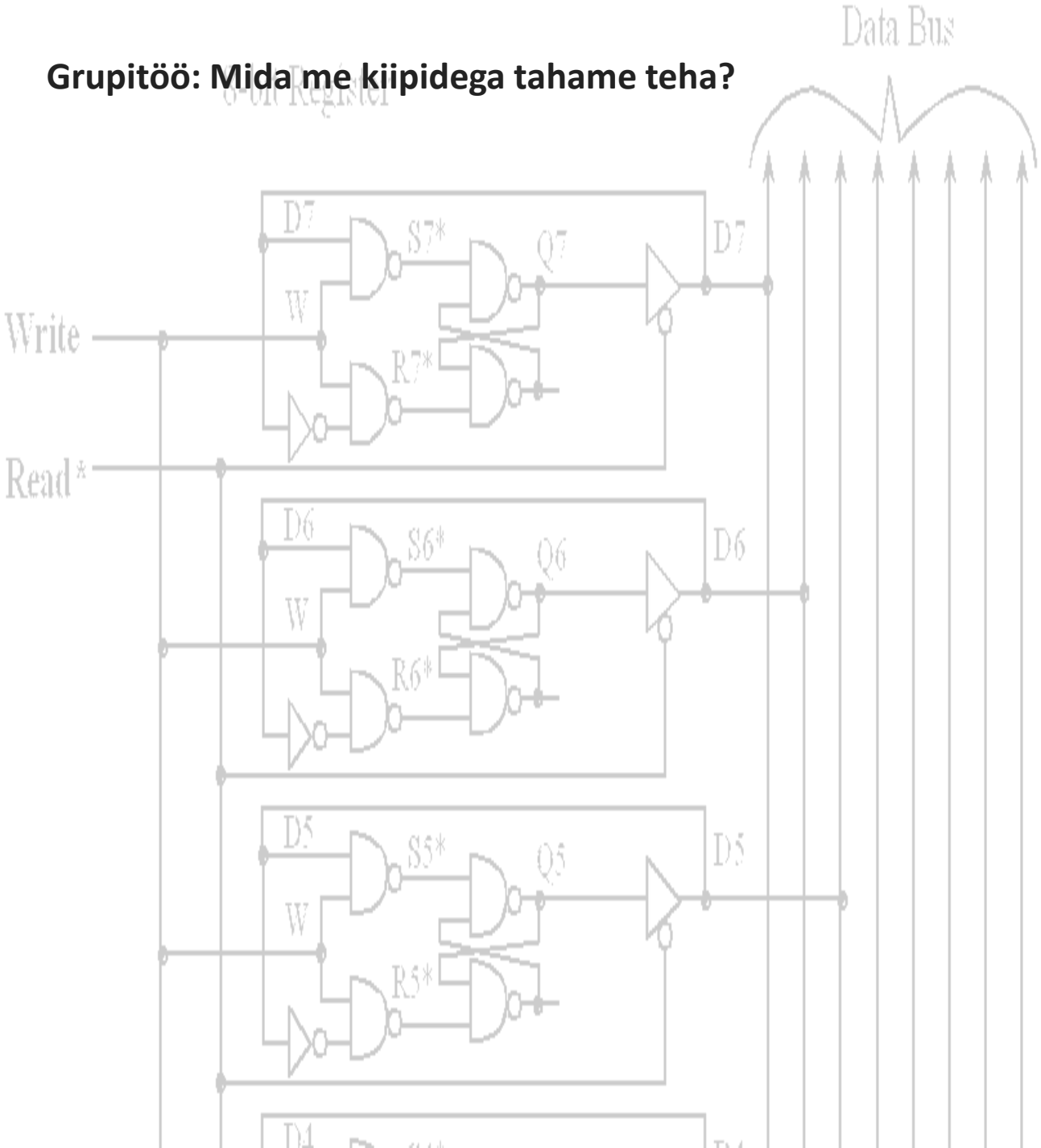
Perioodilise binaarsignaali sagedus arvutatakse valemiga:
f = 1/T, milles f (Hz) ja T (sek).
Käidutsükkel arvutatakse valemiga: Duty cycle = (t_w/T) x 100%


OLD WAY
NEW WAY

Signaale saab teisendada.

Selleks kasutatakse praktikas loogilisi elemente ja selle registreerimiseks kasutatakse formaalselt loogilisi funktsioone.

Grupitöö: Mida me kiipidega tahame teha?



- Selgita “Digital logic circuits can be broken down into two subcategories- **combinational** and **sequential**.”
- Too mõlema kohta näited päris elust

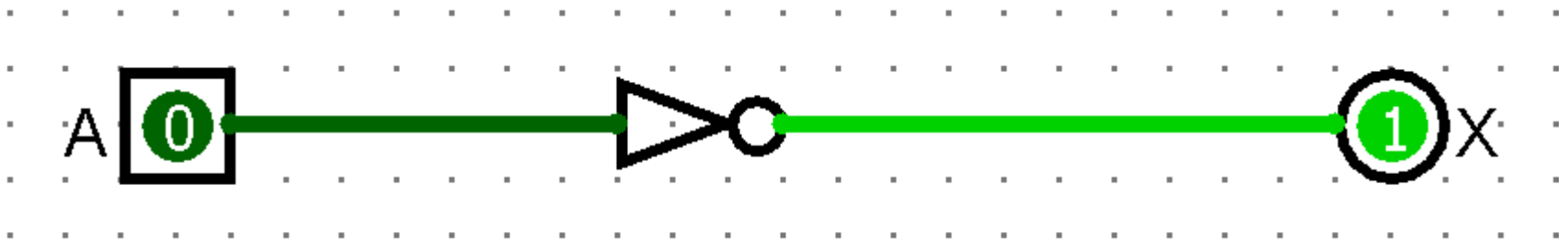
TRUE = 1

FALSE =0

Signaale saab teisendada.

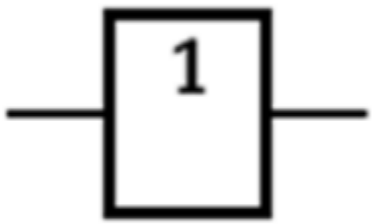
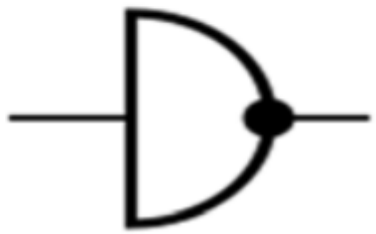
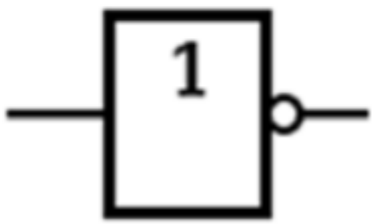
Selleks kasutatakse praktikas loogilisi elemente ja selle registreerimiseks kasutatakse formaalselt loogilisi funktsioone.

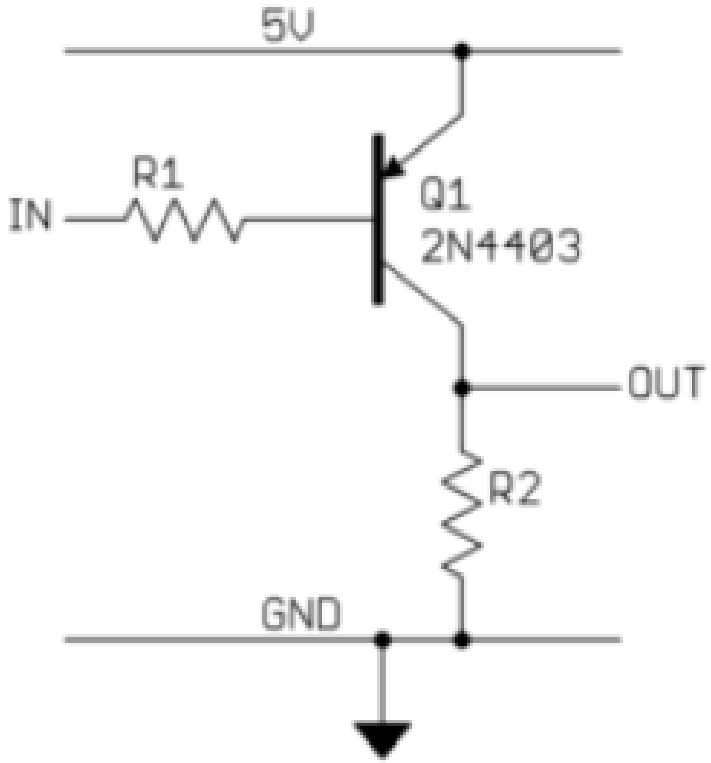
Negatsioon - pöörab signaali ümber.

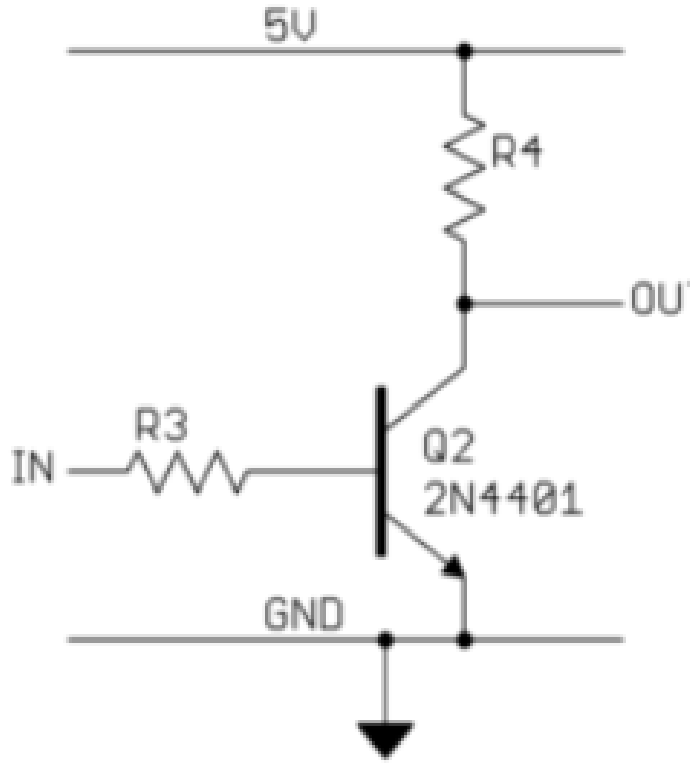


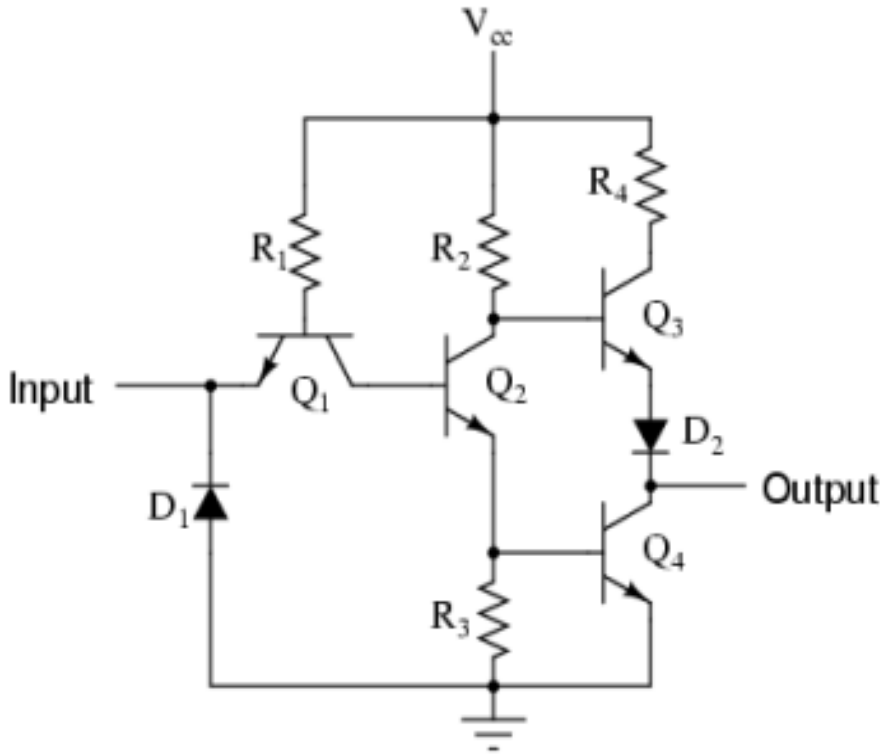
Sisend (A)	Väljund (X)
1	0
0	1

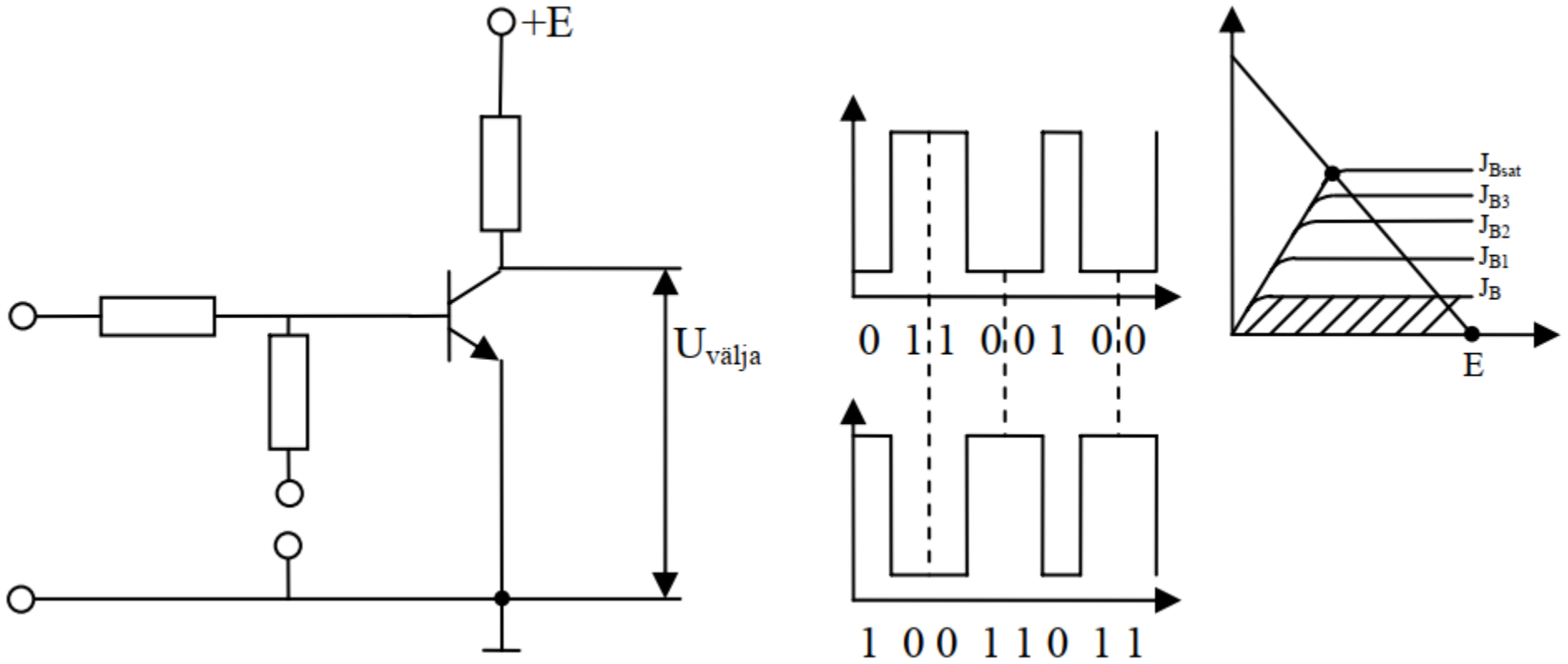
A	X
0	1
1	0

Nimetus	ANSI/IEEE Std 91, 91a	IEC 60617	DIN 40700	EN 60617 (kehtetu)
Puhver (Buffer)				
EI (NOT)				


5V
R1
IN
Q1
2N4403
OUT
R2
GND

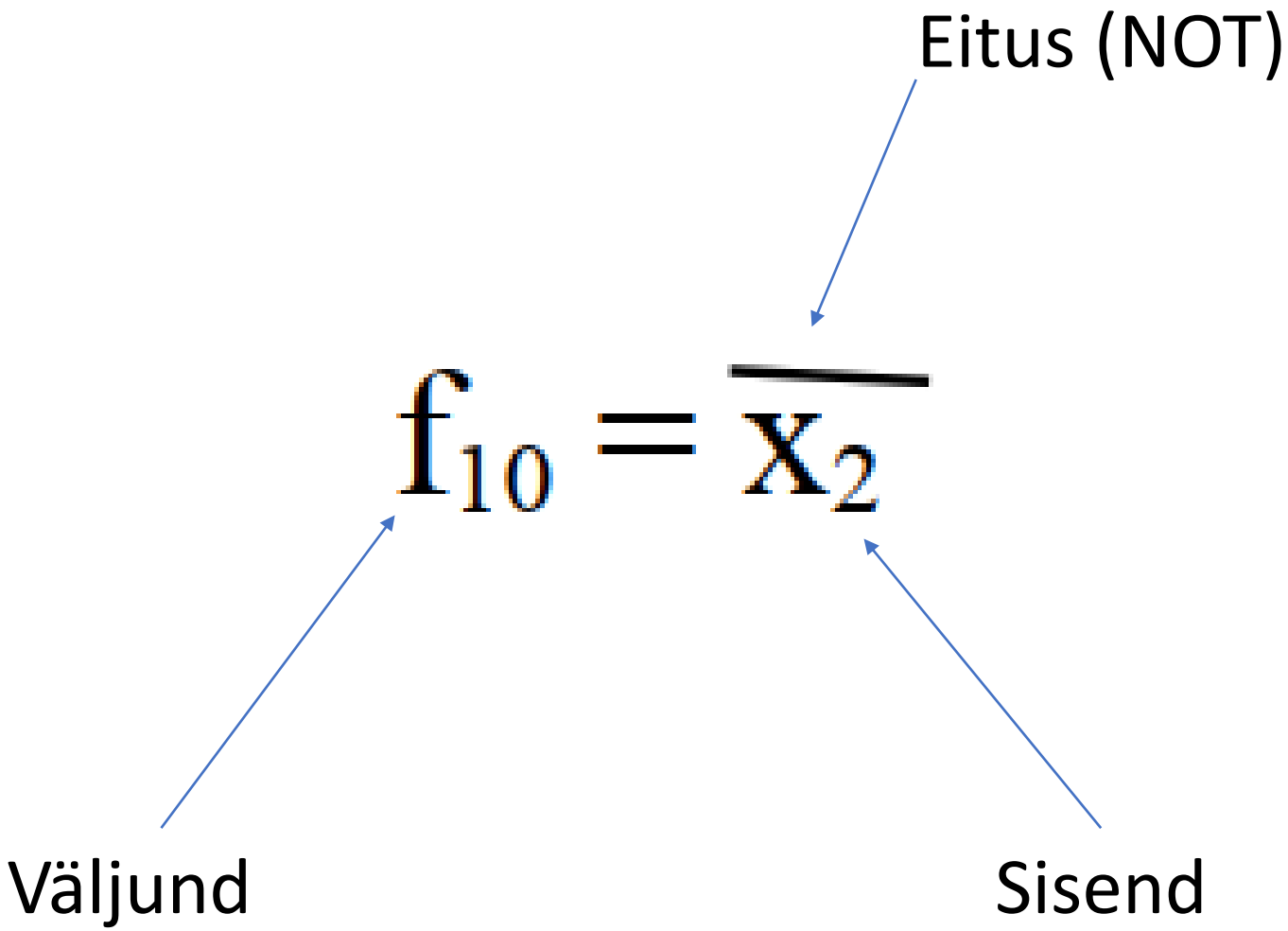

5V
R4
OU
R3
IN
Q2
2N4401
GND


Vcc
R1
R2
R4
Q3
Input
Q1
Q2
D2
Output
D1
Q4
R3

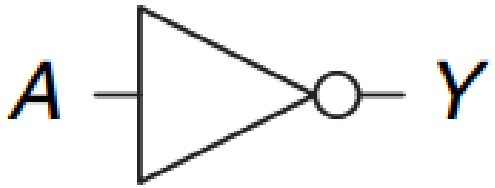


Kui sisendis on madal potentsiaal ehk loogiline 0, siis on transistor sulgrežiimis. Tema kollektori pinge on suur UCE~E st väljundis on loogiline 1. Kui sisendis on kõrge potentsiaal ehk loogiline 1, siis töötab transistor küllastus režiimis kollektori pinge on väike UCE~E st väljundis on loogiline 0

Väljund võrdub sisendi eitusega



NOT



$$Y = \overline{A}$$

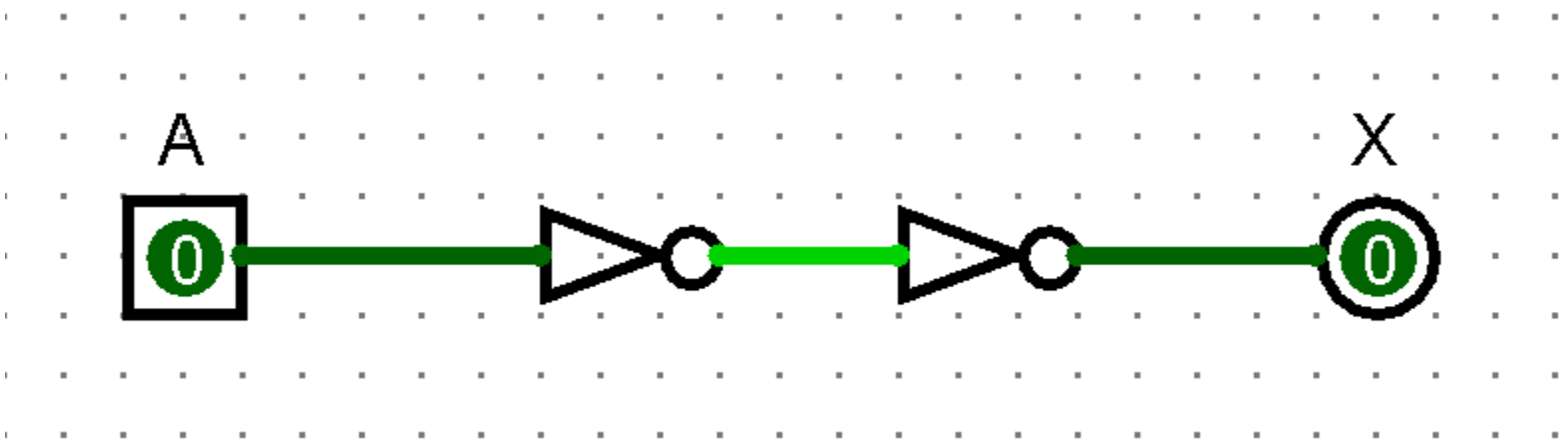
A	Y
0	1
1	0

karnaugh table

$Y = \overline{A}$ is read "Y equals NOT A."

Eituse eitamise seadus. Argumendi väärtus tema kahekordsel eitamisel ei muutu

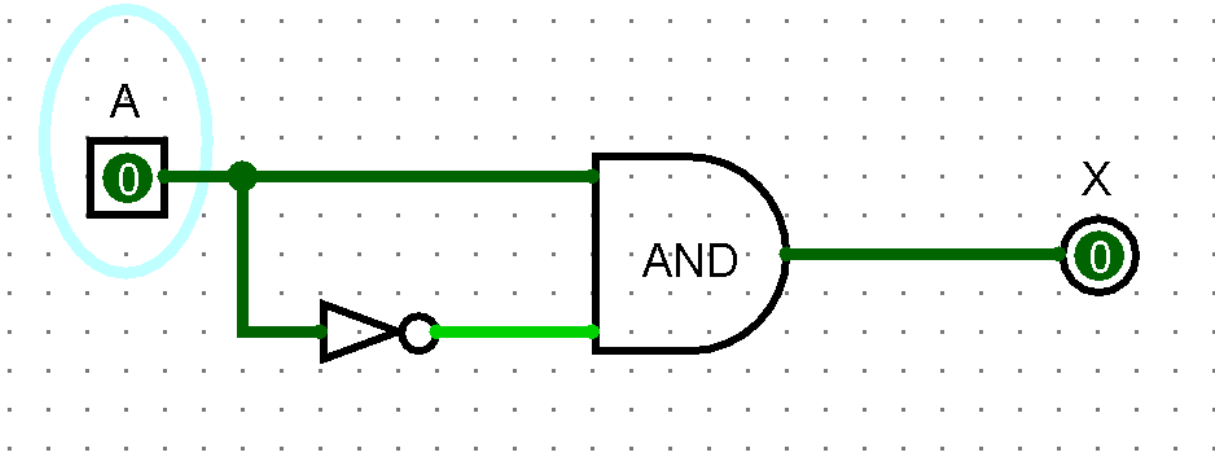
$$\overline{\overline{a}} = a$$



A	X
0	0
1	1

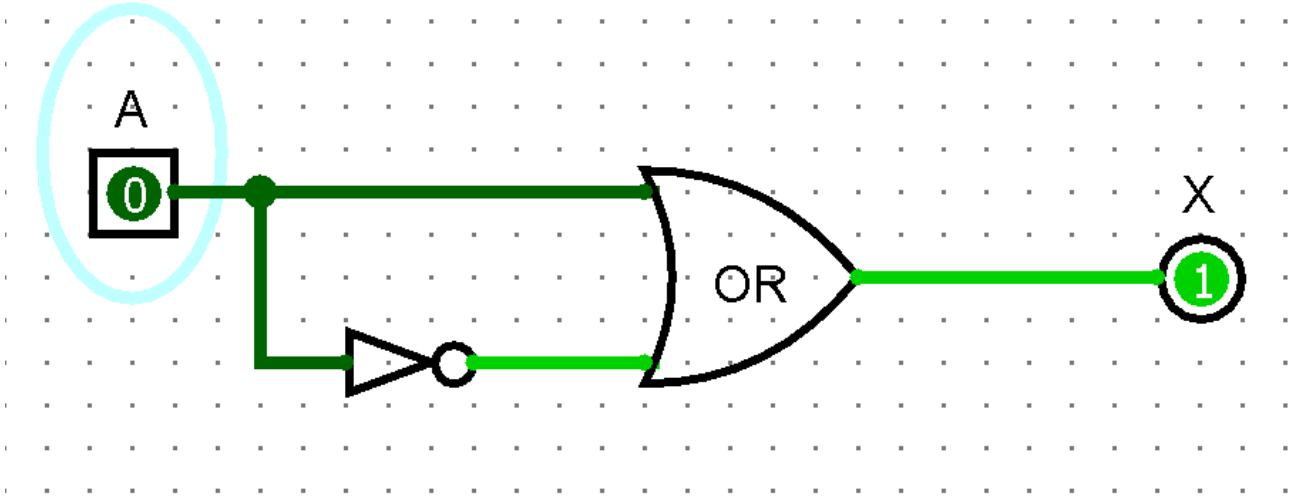
Komplementaarsus-ehk täiendiseadus. Argumendi ja tema eituse ehk täiendi loogiline korrutis on null, loogiline summa üks.

$$a \cdot \bar{a} = 0$$

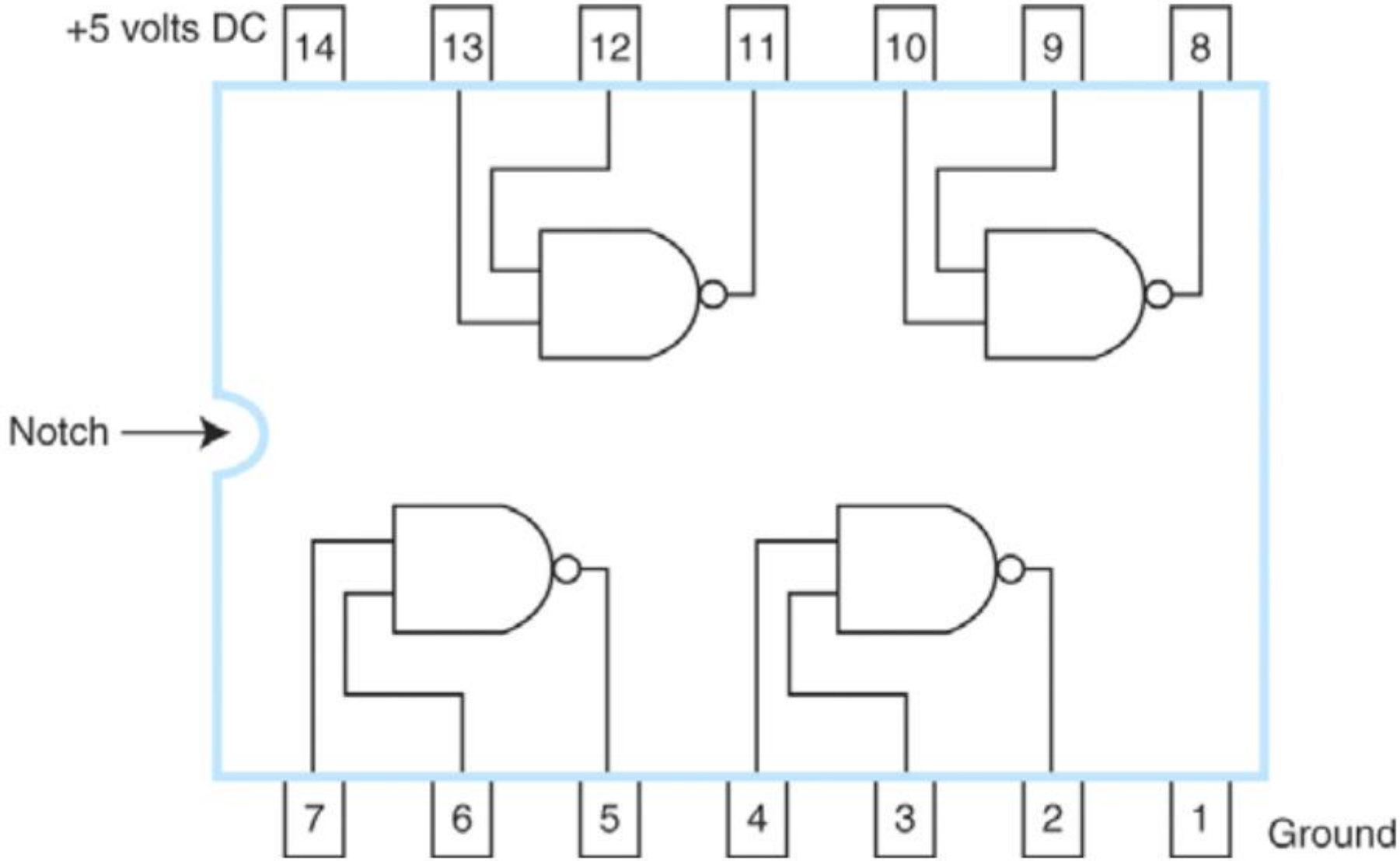


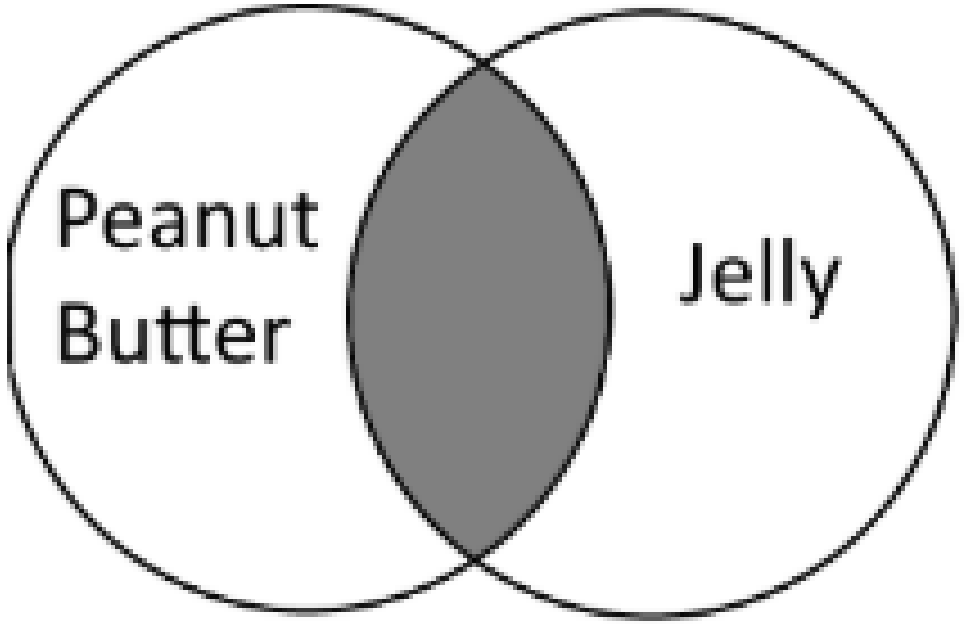
A	X
0	0
1	0

$$a + \bar{a} = 1$$



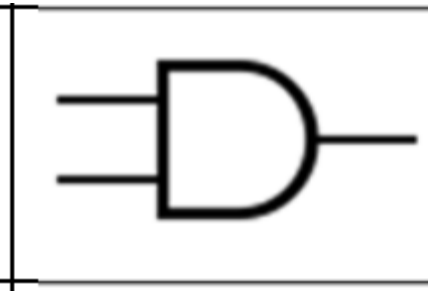
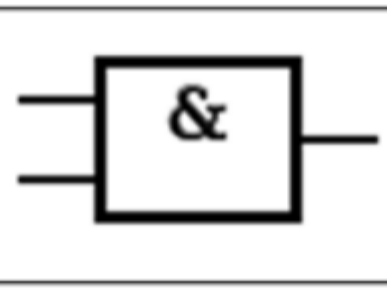
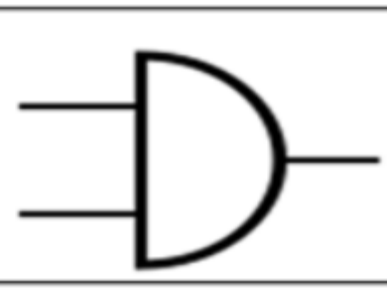
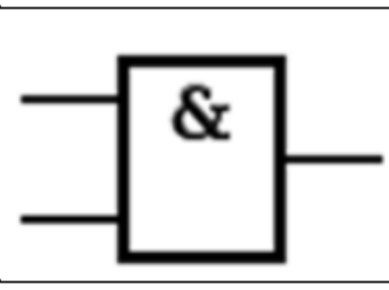
A	X
0	1
1	1

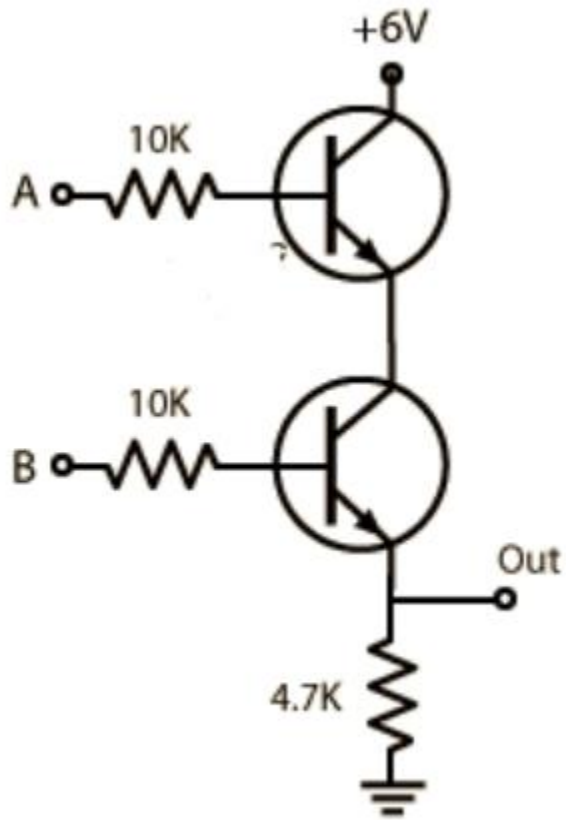

+5 volts DC
14
13
12
11
10
9
8
Notch
7
6
5
4
3
2
1
Ground

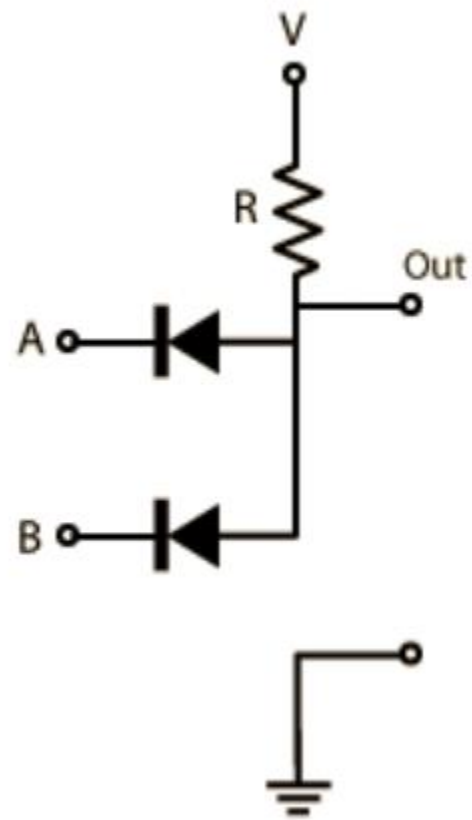


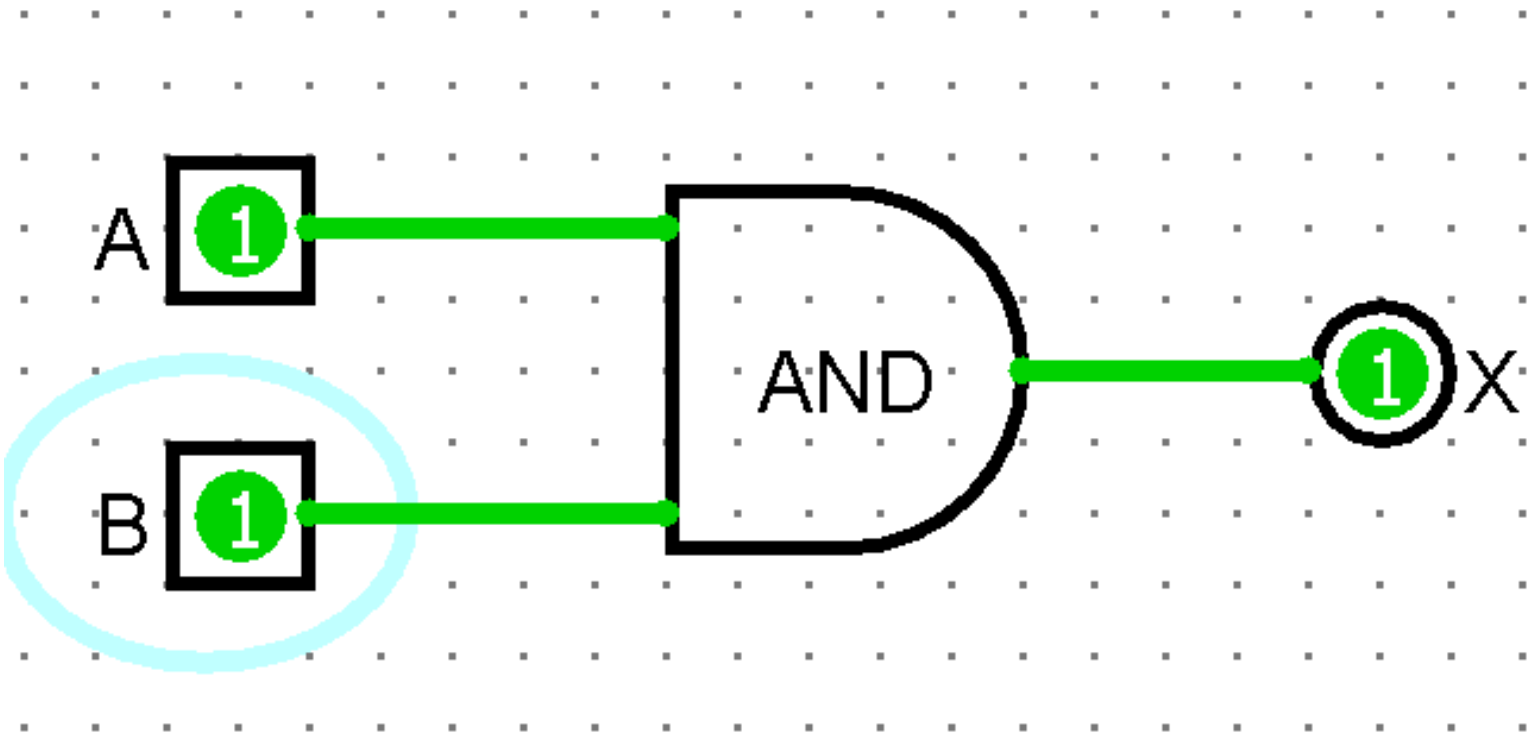
AND

Using AND, this search would only retrieve results with Peanut Butter and Jelly.

Nimetus	ANSI/IEEE Std 91, 91a	IEC 60617	DIN 40700	EN 60617 (kehtetu)
NING (AND)				

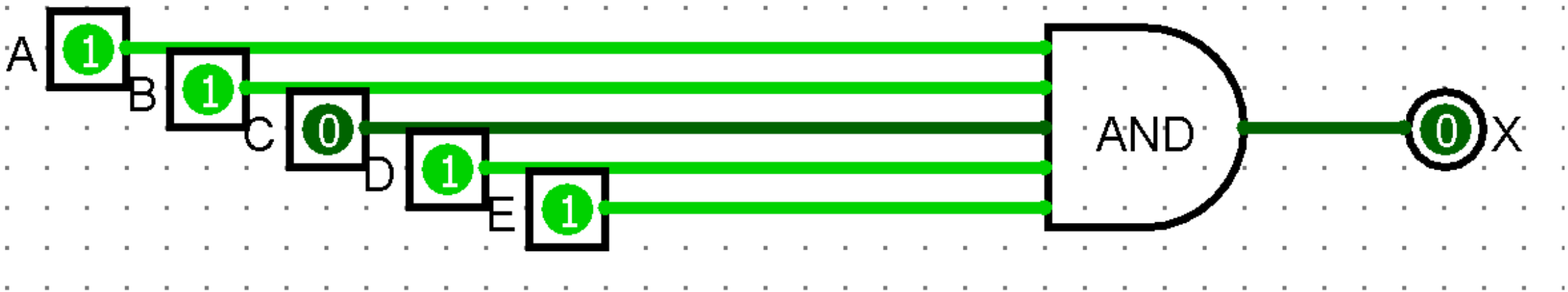

+6V
10K
A
10K
B
Out
4.7K


V
R
Out
A
B



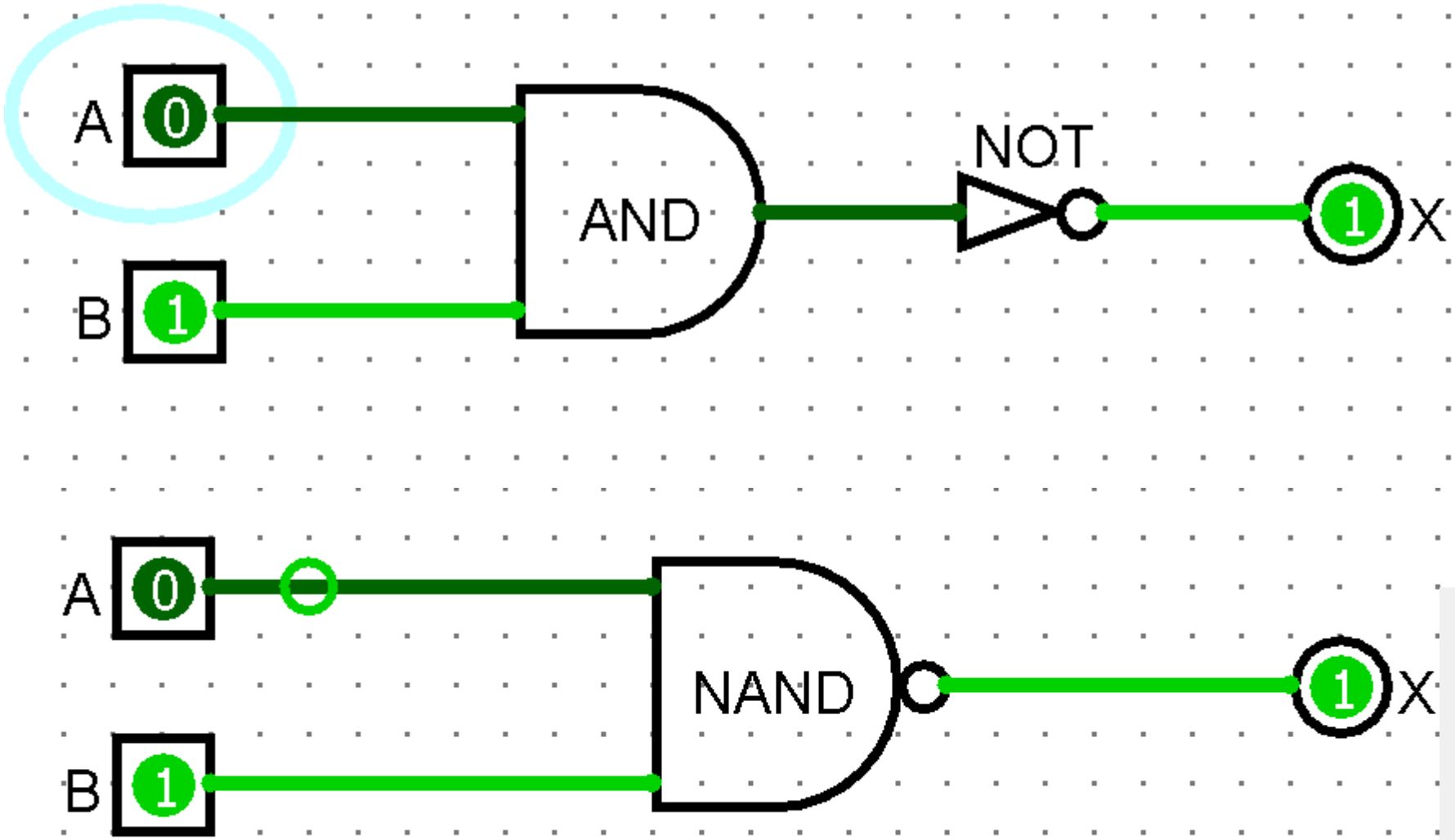
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

Domineerimisseadus I. Suvalise muutujate hulga konjunktsioon on null (tühihulk),
kui kas või ainult üks muutujatest võrdub nulliga
0 • a • b • c •… = 0

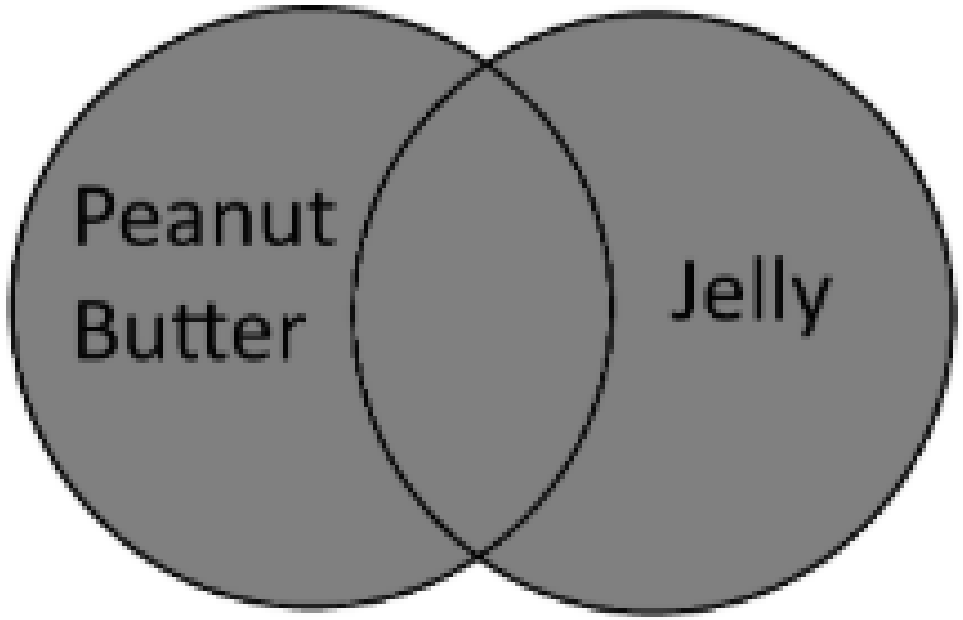


A	B	C	D	E	X
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	0
1	0	1	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	1

AND+NOT = NAND (Ning-Ei)

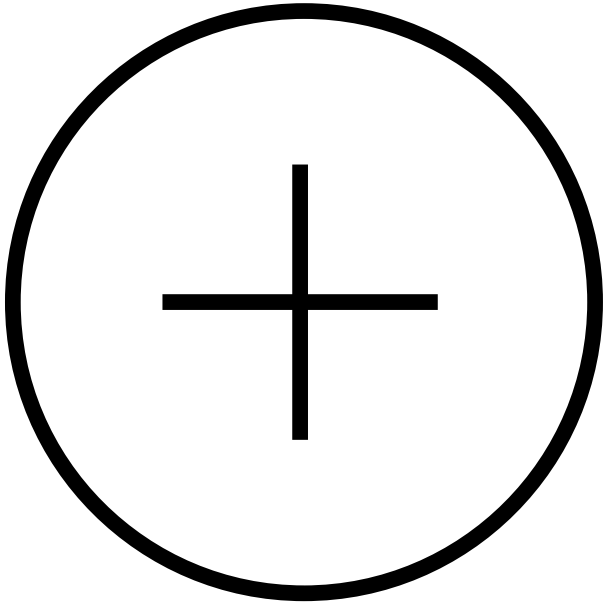


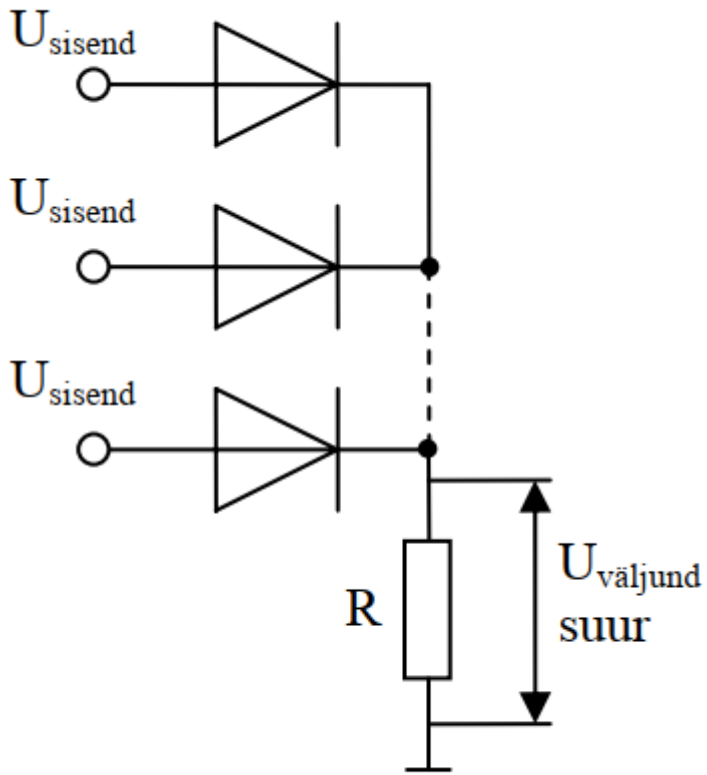
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0



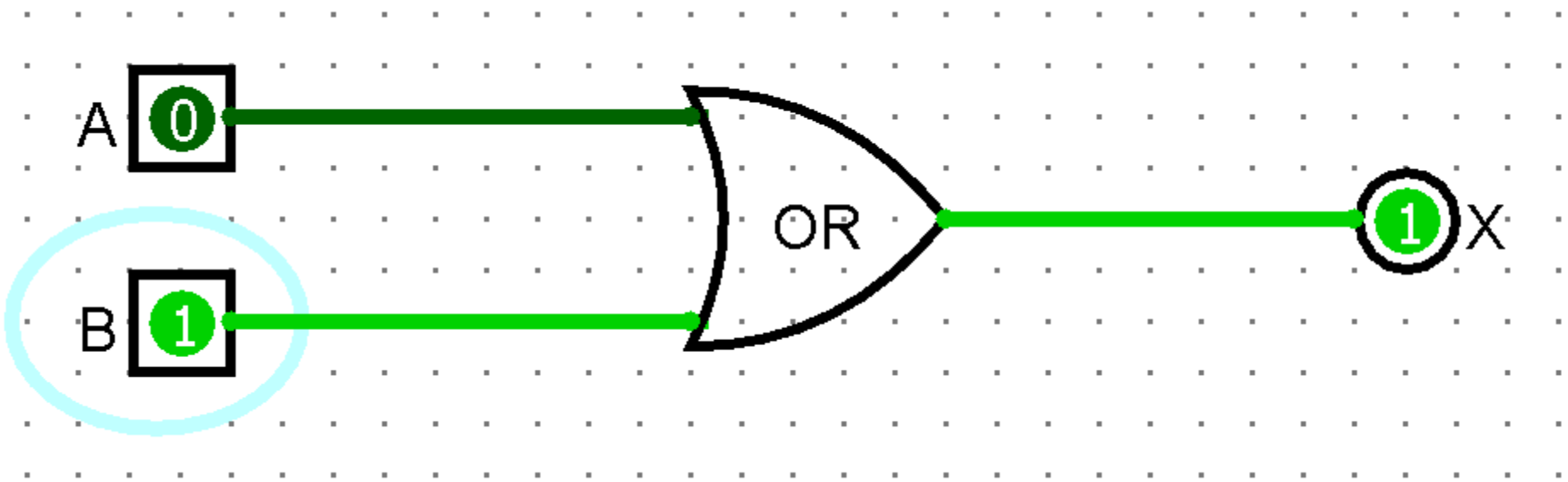
OR

Using OR, this search would retrieve results with peanut butter, with jelly, and with both.



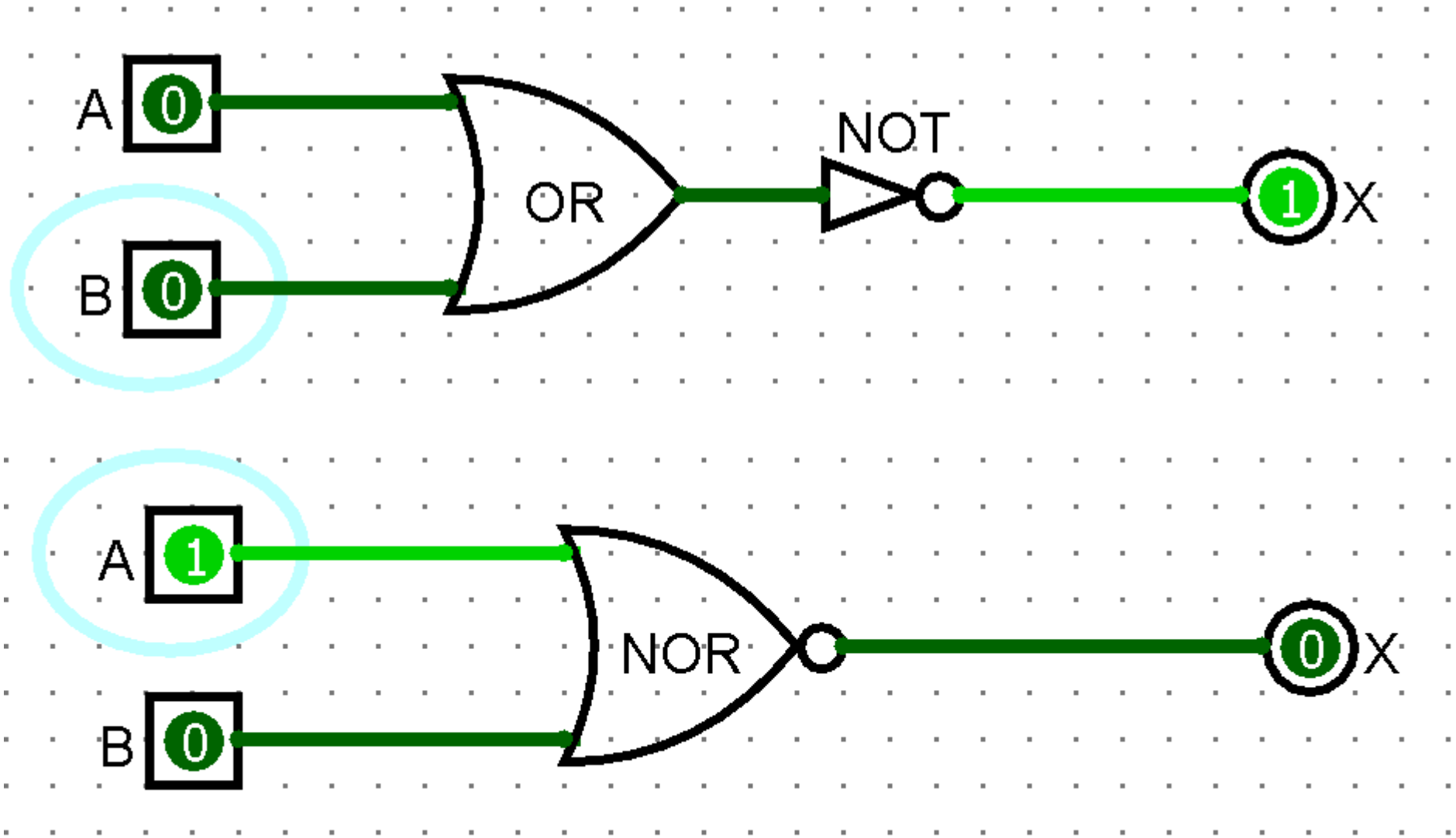


Kui mõnes sisendis on loogiline 1 (impulss või kõrge potentsiaal), siis vastav diood avaneb ja vool läbib avanenud dioodi ja takistit R. Takistil tekib kõrge pinge ehk loogiline 1. Ükskõik mitmest sisendis on loogiline üks on väljundis sammuti loogiline üks. Kui RF on tunduvalt väiksem kui R, siis on väljundpinge võrdne sisendpingega olenemata avanenud dioodide arvust. Kui kõikides sisendites on 0 siis on kõik dioodid suletud ja väljundis on 0.



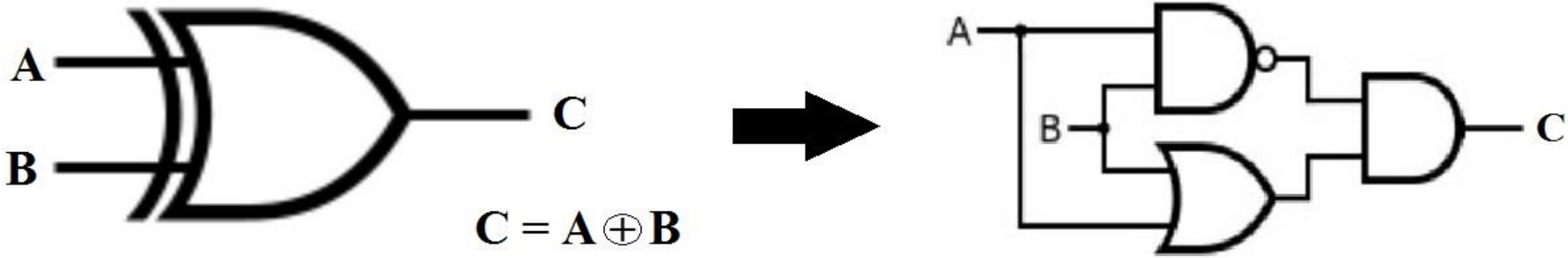
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

OR+NOT=NOR (Ning-Ei)



A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate



Output — C = A⊕B — Input 1, Input 2

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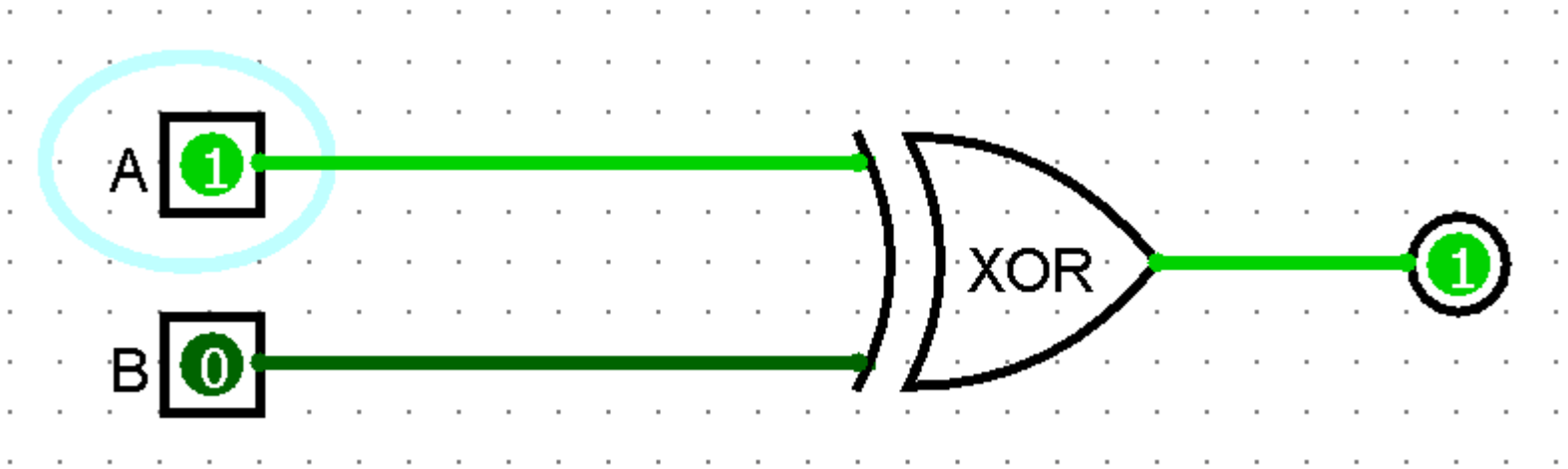
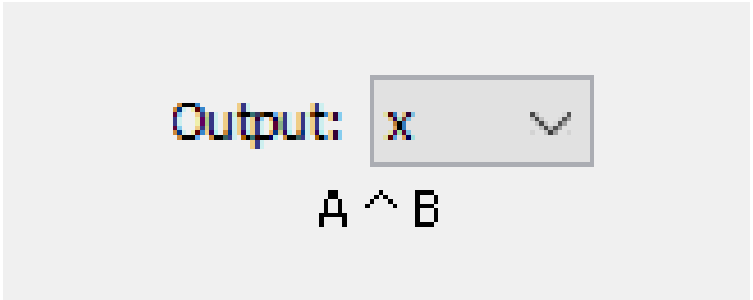
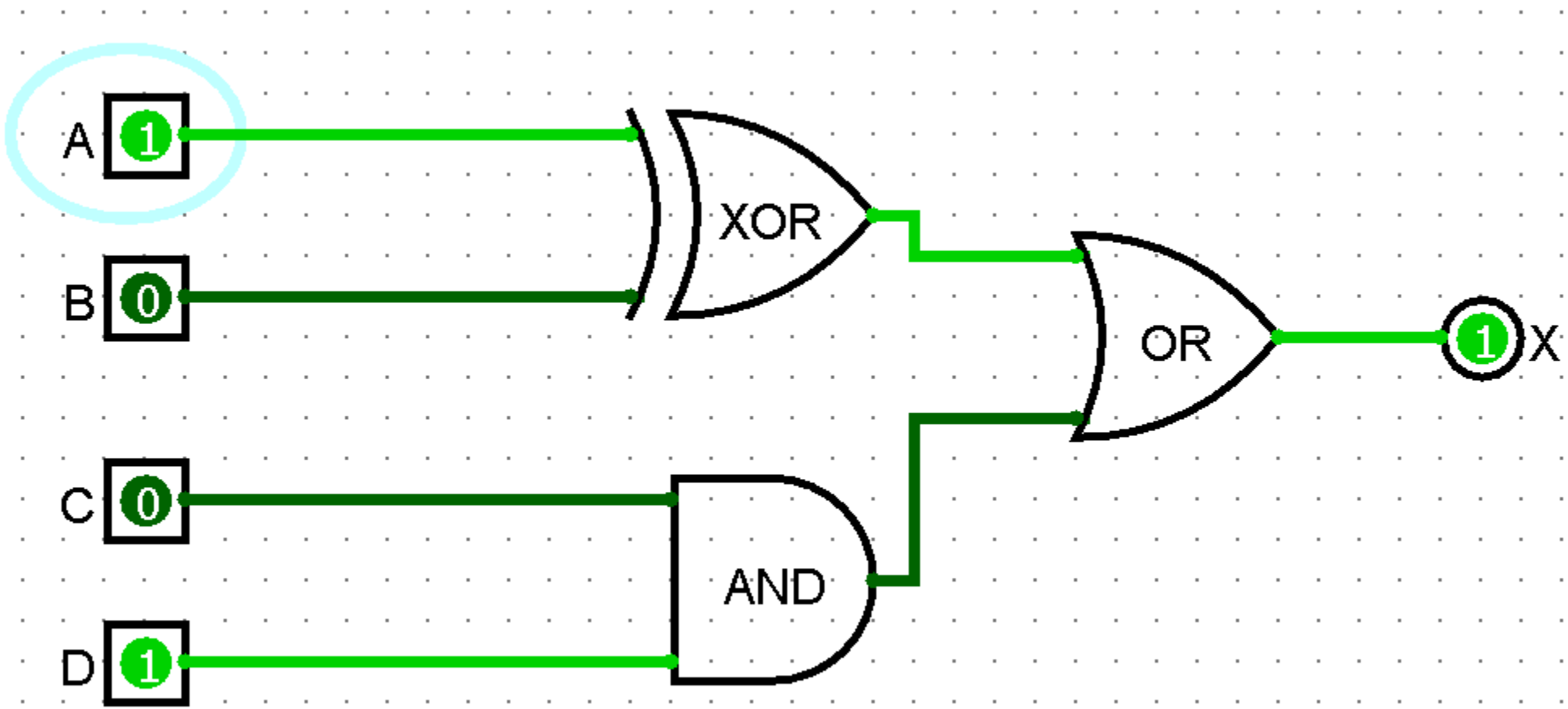
XORi puhul kui on erinevad sisendid, siis väljundiks 1



A	B	x
0	0	0
0	1	1
1	0	1
1	1	0



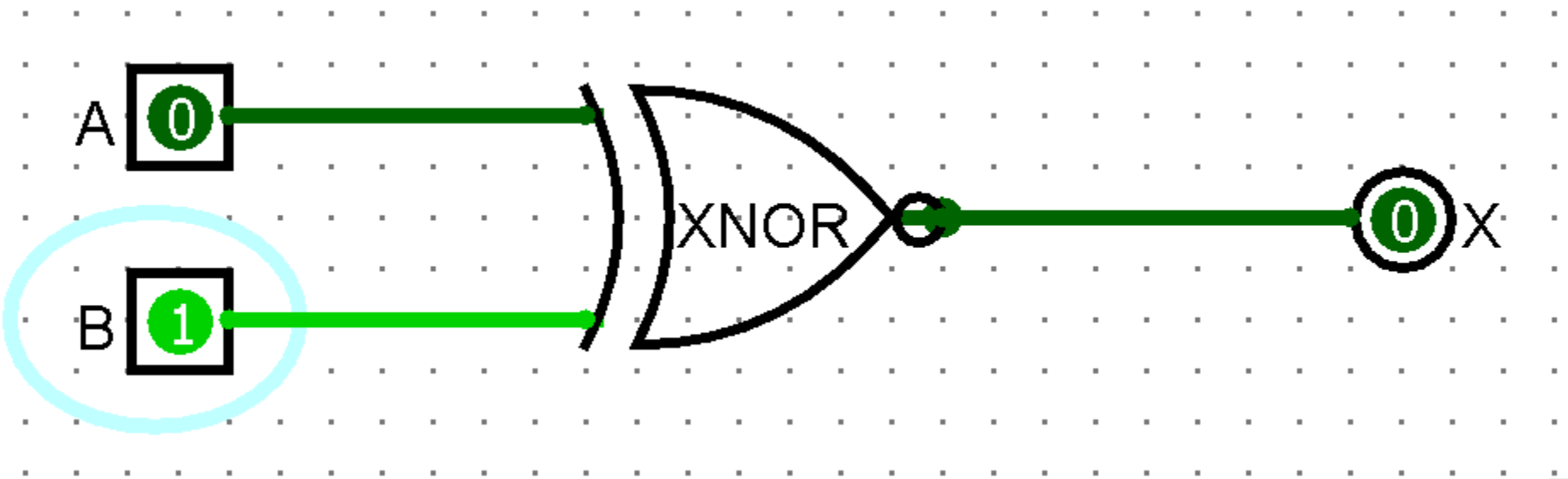

A
1
B
0
C
0
D
1
XOR
AND
OR
1
X

Output: X

A ^ B + C D

A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Ekvivalents (XNOR) on loogikafunktsioon, mis võrdub ühega kui argumendid on sama väärtusega.

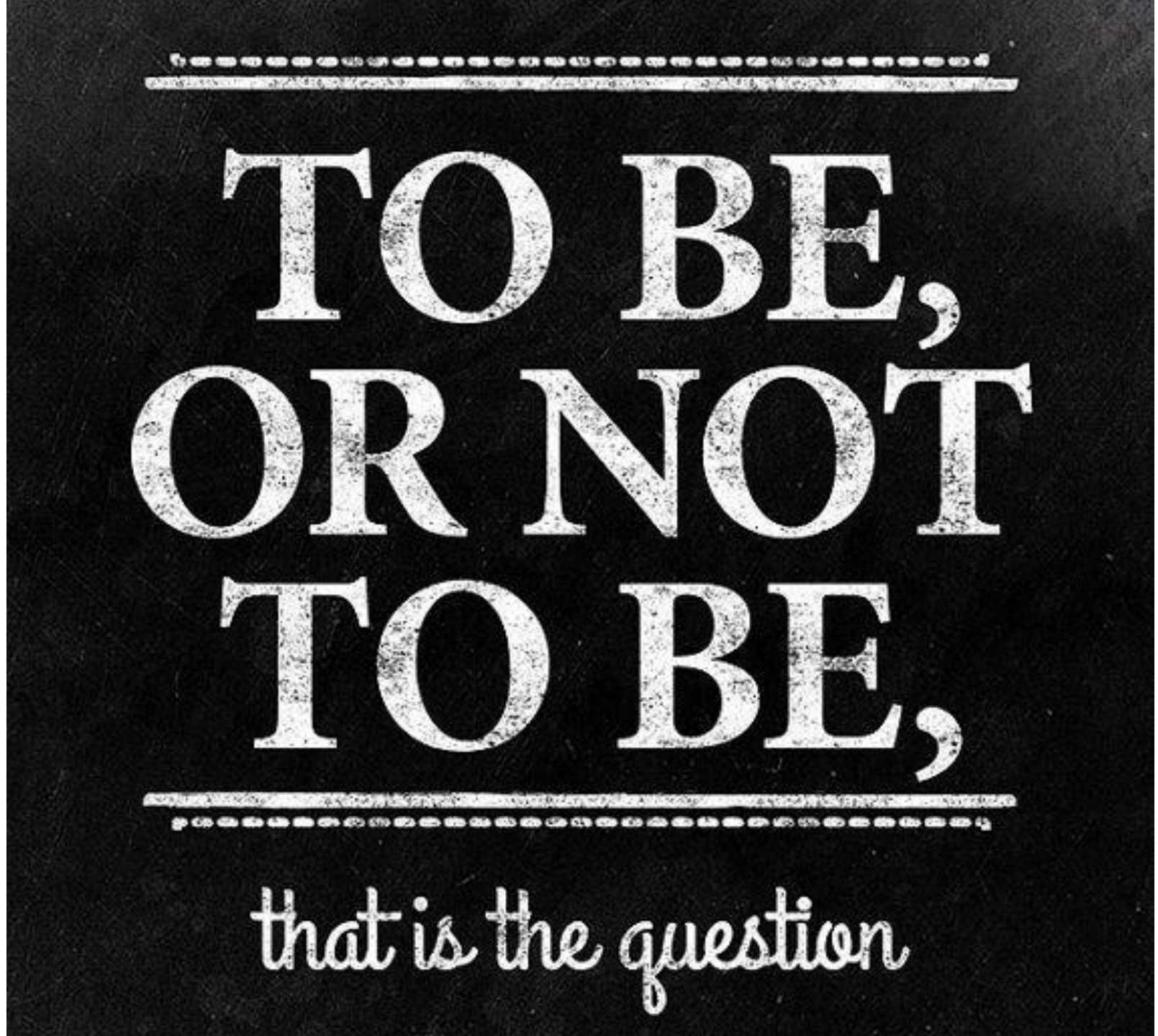


A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

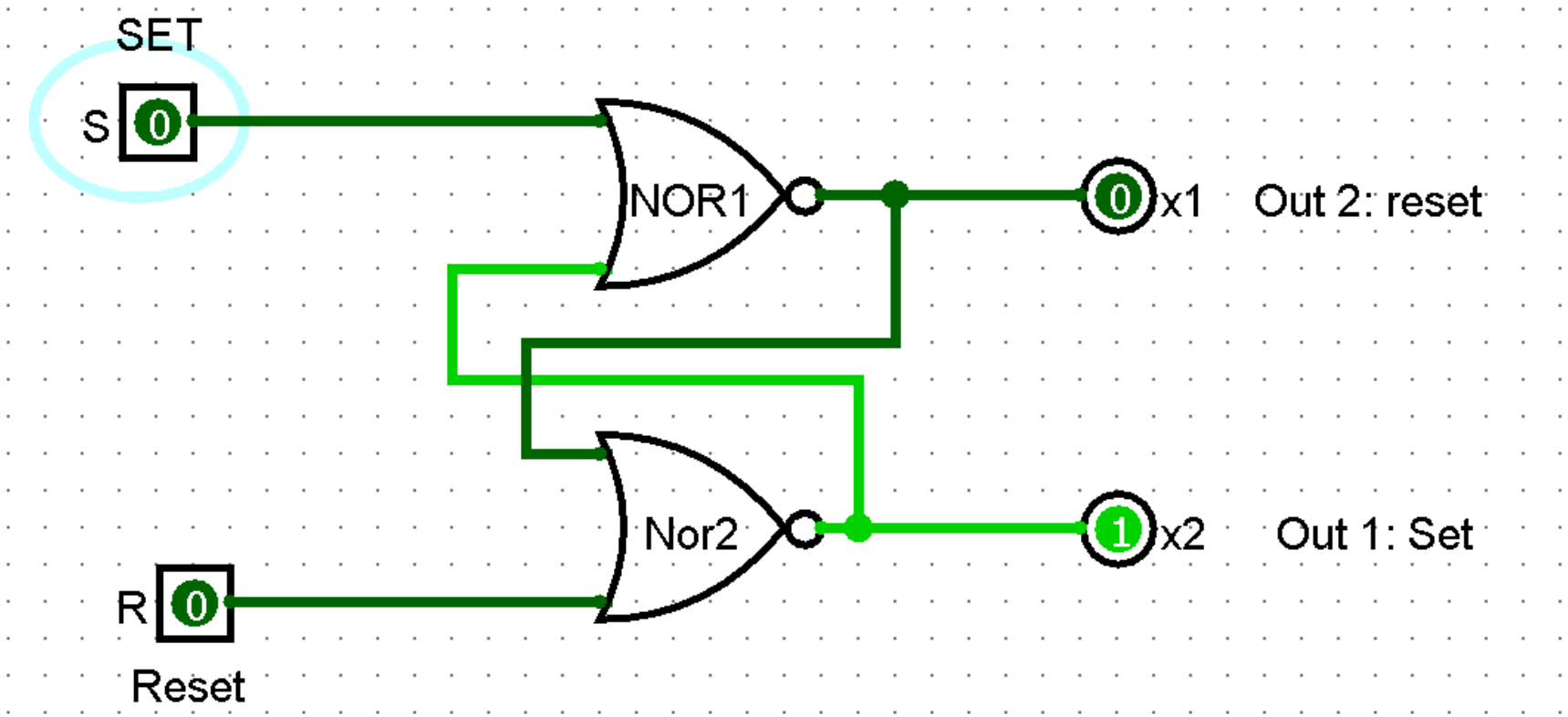
Output: X

$\overline{A \wedge B}$

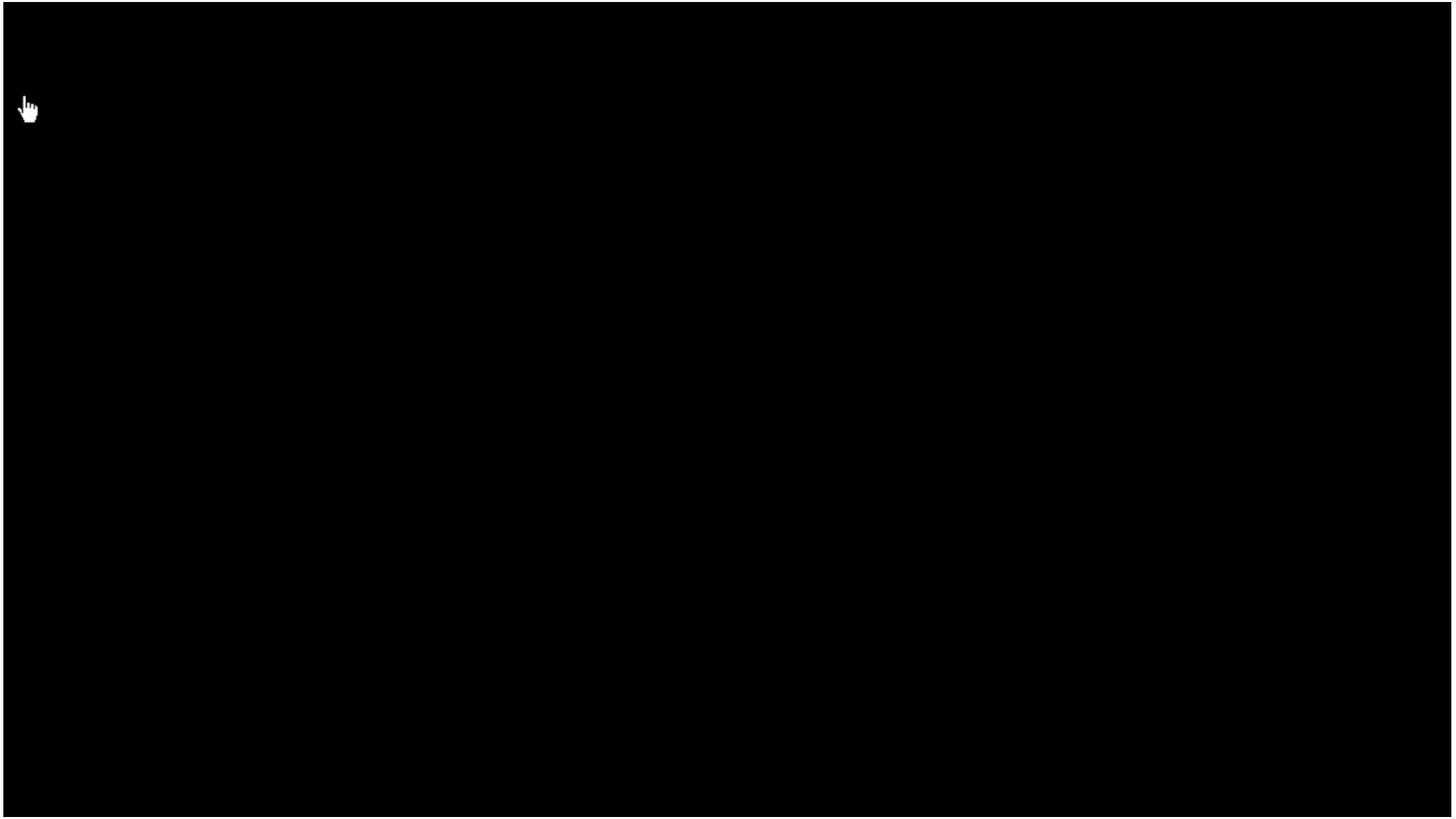
24.10.2022


TO BE,
OR NOT
TO BE,
that is the question

Asünkroonne

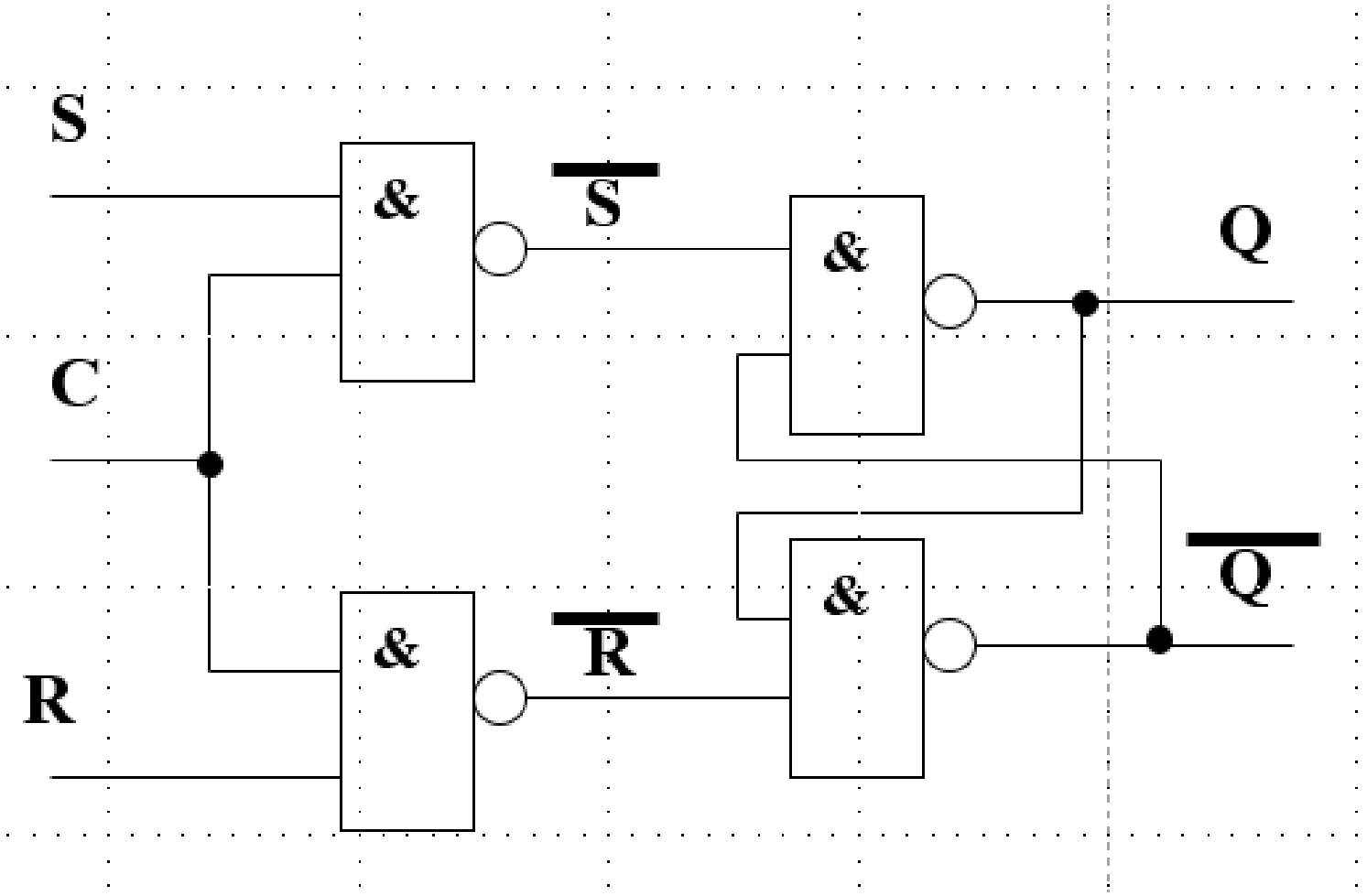


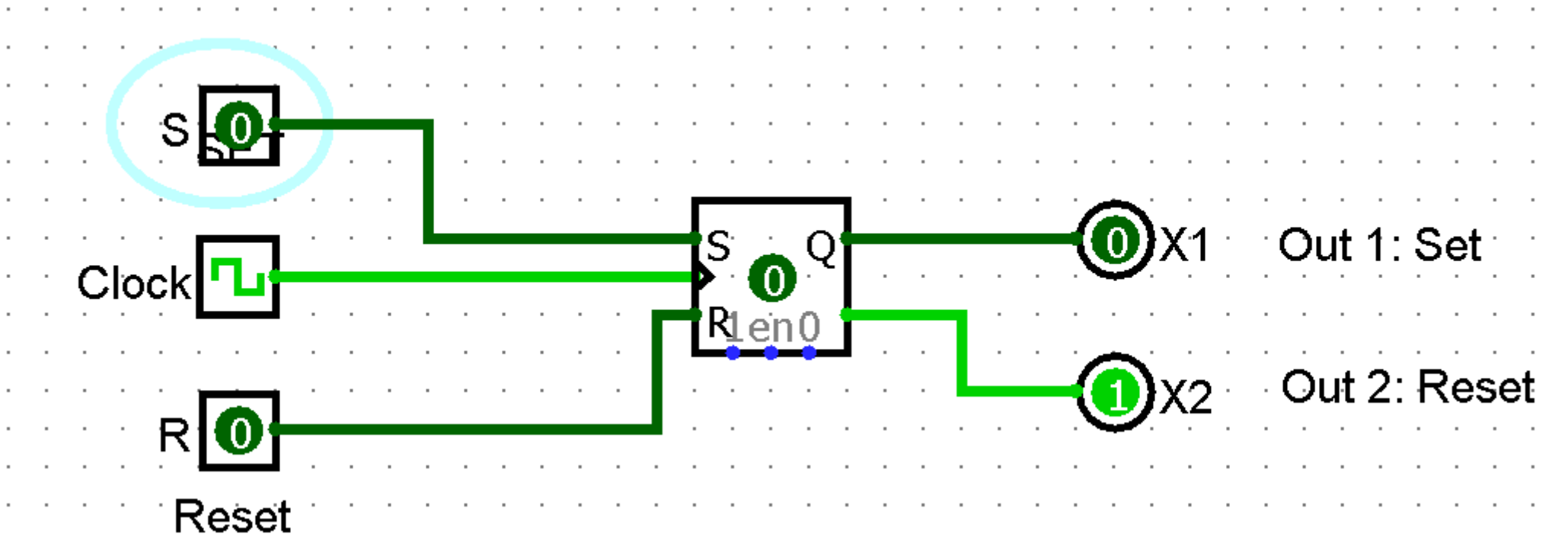
S	R	x1	x2
0	0	0	0
0	1	1	0
1	0	0	1
1	1	0	0



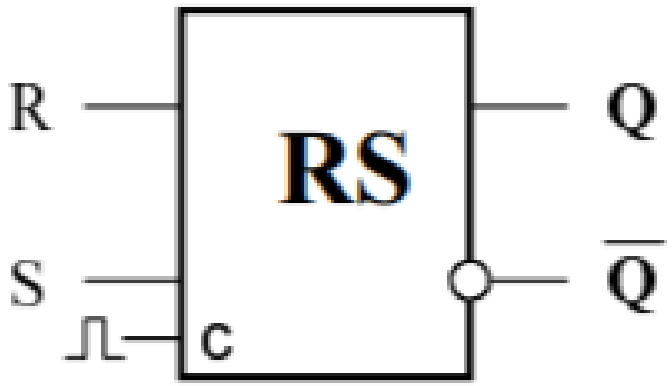
„Triger on mäluelement mis säilitab 1bit informatsiooni.“

Sünkroonne SR triger




S
0
Clock
R
0
Reset
S
Q
0
R
1en0
0
X1
Out 1: Set
1
X2
Out 2: Reset

RS-trigeri töötabel:



R	S	Q_{n+1}
0	**0**	Q_n
0	**1**	**1**
1	**0**	**0**
1	**1**	×

ehk

Q_n	Q_{n+1}	R	S
0	**0**	—	**0**
0	**1**	**0**	**1**
1	**0**	**1**	**0**
1	**1**	**0**	—

R — RS-trigeri ergutussignaal *"reset"*

S — RS-trigeri ergutussignaal *"set"*

RS-trigerit ei tohi juhtida ergutussignaalide paariga **R = 1** **S = 1**

(ei saa käskida trigerit nii olekusse **0** kui ka **1** samaaegselt)

- Latch – võib muuta oma väljundit mitmel korral kui taktsignaal on kõrge.

- Flip-flop – muudab oma väljundit AINULT siis, kui toimub taktsignaali oleku muutus.